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Advancing the Frontiers of Green Technologies

TUTORIALS
Abstract:
Designing analog circuits on deep sub-micron process technologies (32, 22, 14, 10, 7, 5 nm) has its own set of challenges. With supply voltage scaling down, threshold voltages holding its values to maintain moderate leakage currents as demanded by low power designs for modern and mobile gadgets, the headroom is running out. Coupled with degraded rout and denser metal stack, stringent design and density rules make analog design even tougher, especially for high yield products that are required to ship hundreds of millions of units with very low wafer cost. This focused tutorial is intended to address these challenges from an industrial view point, starting from the basics, building its way up to designing advanced analog blocks in deep submicron process nodes, while keeping yield as the number one challenge.

Instructor(s):
Ahmed Helmy, Associate Professor, Dept. of Electrical & Computer Engineering, Arizona State University, Senior Staff Design Manager, Intel Corporation, Chandler, Arizona, USA.

Ahmed Helmy received his Bachelor degree in electrical and electronics engineering from Ain Shams University Cairo Egypt in 1994, masters in engineering physics and mathematics 1999 from the same University. He received his Ph.D. degree in RF circuit design from the Ohio state university in 2006 electrical and computer engineering department. On the industrial level he joined Mentor Graphics Co. Cairo office in 1996 where he worked for four years in macro modeling and behavioral modeling for RF circuits and systems as well as statistical modeling and DFM simulations. He joined Intel Corporation in Arizona in 2002 as an RF circuit designer. Currently he is a Sr. staff design Manager with Intel Corporation working on high speed IO circuits and deep sub-micron process technologies that support such applications. Ahmed is part of the hard IP team that developed Intel icore3/5/7, has many products in the market on 32 and 22nm process nodes. He is also an Associate Professor with Arizona State University since 2008 teaching advanced Analog design. He has several US patents, several publications and a monogram on substrate noise coupling in RFICs. He serves as a reviewer for several IEEE conferences and journals.
Tutorial #2

Frequency Agile Circuits for Multiband and Multimode RF Applications

Abstract:
The trend and demand in wireless communication for an integrated multi-standard transceiver which provides access to various services is a driving force for the development of flexible radio frequency CMOS transceiver building blocks. This tutorial will focus on the challenge of designing highly frequency agile analog RF front-ends, specifically this tutorial will focus on current circuit-level methods and techniques for realizing multiband, frequency agile low noise amplifiers and power amplifiers. A discussion of frequency generation in these types of systems will also take place with a focus on the circuit-level realization of voltage controlled oscillators with ultra-wide tuning ranges.

Instructor(s):
Nathan M. Neihart, Assistant Professor, Dept. of Electrical & Computer Engineering, Iowa State University, Ames, Iowa, USA.

Nathan M. Neihart received both the B.S. and M.S. degrees in Electrical and Computer Engineering from the University of Utah, Salt Lake City, in 2004. He received the Ph.D. degree in Electrical Engineering from the University of Washington, Seattle, in 2008, where he received the Analog Devices Inc., Outstanding Student Designer Award in 2007. In 2008 he joined Iowa State University, Ames, where he is now an Assistant Professor of Electrical and Computer Engineering. His research interests include reconfigurable RF circuits and systems for multi-band/multi-mode and cognitive radios, circuits and systems for multiple-input multiple-output transceiver, and the fabrication and applications of memristors. From 2010 to 2012, Dr. Neihart served as an Associate Editor for the IEEE Transactions on Circuits and Systems-II: Express Briefs. Since 2012, Dr. Neihart has served as an Associate Editor for the IEEE Transactions on Circuits and Systems-I: Regular Papers. Dr. Neihart also serves on the technical program committee for IEEE International Symposium on Circuits and Systems.

Abstract:
This tutorial presents a comprehensive description of behavioral modeling and simulation techniques, showing how to implement these techniques in an efficient way using MATLAB/SIMULINK. The methodology described in this tutorial is based on the use of the so called C-coded SIMULINK S-functions to develop precise models of analog circuits, which allow designers to simulate complex systems with reduced simulation time, while keeping high accuracy. This simulation approach can be combined with an optimizer to automate the high level synthesis and verification of many different analog integrated systems. As an application, two different toolboxes developed using the proposed techniques are illustrated in this tutorial: one is intended for the simulation of wireless receivers and the other one focuses on ΣΔ data converters. Through the multiple examples included in these toolboxes, tutorial attendees will get inside into the philosophy behind the presented approach and will learn how to apply it to their own designs and projects.

Instructor(s): 
Jose M. de la Rosa, Associate Professor, 
Instituto de Microelectrónica de Sevilla, IMSE-CNM 
Parque Tecnológico de la Cartuja, C/ Américo Vespucio 
41092 – Sevilla, SPAIN.

Jose M. de la Rosa, IEEE Senior Member, received the M.S. degree in Physics in 1993 and the Ph.D. degree in Microelectronics in 2000, both from the University of Seville, Spain. Since 1993 he has been working at the Institute of Microelectronics of Seville (IMSE), which is in turn part of the Spanish Microelectronics Center (CNM) of the Spanish National Research Council (CSIC). He is also with the Department of Electronics and Electromagnetism of the University of Seville, where he is currently an Associate Professor. His main research interests are in the field of analog and mixed-signal integrated circuits, especially high-performance data converters, including analysis, behavioral modeling, design and design automation of such circuits. In these topics, Dr. de la Rosa has participated in a number of National and
European research and industrial projects, and has co-authored more than 170 international peer-reviewed publications, including journal and conference papers, book chapters and the books Systematic Design of CMOS Switched-Current Bandpass Sigma-Delta Modulators for Digital Communication Chips (Kluwer, 2002), CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom: Error Analysis and Practical Design (Springer, 2006), Nanometer CMOS Sigma-Delta Modulators for Software Defined Radio (Springer, 2011) and CMOS Sigma-Delta Converters: Practical Design Guide (Wiley-IEEE Press, 2013). Dr. de la Rosa is a member of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society. He serves as Associate Editor for IEEE Transactions on Circuits and Systems I: Regular Papers. He has also served and is currently serving as a review committee member of IEEE ISCAS conference. He participated and is currently participating in the organizing and technical committees of diverse international conferences, among others IEEE MWSCAS, IEEE ICECS, IEEE LASCAS, IFIP/IEEE VLSI-SoC and DATE. He served as TPC co-chair of IEEE MWSCAS 2012 and IEEE ICECS 2012. He is also a member of the Steering Committee of IEEE MWSCAS.
Tutorial #4

Power Management Circuits for Low-Power Applications

Abstract:

Developing power management schemes for low power mixed-signal applications require engineers with solid background in conventional power converter design. Since power converters are rarely covered in graduate or undergraduate circuits’ curriculum, there is a serious shortage in researchers and engineers who have the necessary background to develop efficient and cost-effective solutions. This tutorial will introduce the basic power management schemes used in low-power mixed-signal systems. This includes system level architectures, and noise coupling mechanisms through power management modules. On the circuit level, the basics of linear regulators, buck regulators, and battery chargers will be covered.

Instructor(s):

Ayman Fayed, Assistant Professor, Dept. of Electrical & Computer Engineering, Iowa State University, Ames, Iowa, USA.

Ayman Fayed received his B.Sc. degree in Electronics & Communications Engineering from Cairo University in 1998, and his M.Sc. and Ph.D. degrees in Electrical & Computer Engineering from The Ohio State University in 2000 and 2004 respectively. From 2000 to 2009, he held several technical positions at Texas Instruments Inc., where he was a key contributor to many product lines for wire-line, wireless, and multi-media devices. From 2000 to 2005, he was with the Connectivity Solutions Dept. at TI, where he led the design of the frontend of high-speed wire-line transceivers such as USB 2.0, IEEE1394b, and HDMI in several nanometer CMOS technology nodes. He also led the design of fully integrated power management solutions for portable media players including different classes of switching/linear regulators and battery chargers. From 2005 to 2009, he was a member of the technical staff with the wireless analog technology center at TI, where he led several projects in 65nm and 45nm CMOS technologies including baseband sigma-delta data converters for GSM/WCDMA/WIMAX standards, and fully integrated power management solutions for mixed-signal SoCs with multi-RF cores. Since 2009, Dr. Fayed has been an assistant professor at the Dept. of Electrical & Computer Engineering, Iowa State University, Ames, Iowa, where he is the founder and director of the Power Management Research Lab (PMRL). His research interests include embedded power management/conversion for RF/mixed-signal SoCs and multi-core processors, energy harvesting for power-restricted and remotely-deployed devices, high-speed wire-line transceivers, and data converters. Dr. Fayed has many publications and patents in the field and has authored a book in the area of adaptive systems titled “Adaptive Techniques for Mixed Signal System On Chip” (Springer 2006). He is a senior member of IEEE and serves in the technical program committee of many IEEE international conferences such as RFIC, ISCAS, and MWSCAS. Dr. Fayed is a recipient of the 2013 National Science Foundation CAREER Award.
Tutorial #5

Wearable Biomedical Sensor Design: Towards Preemptive and Proactive Healthcare

Abstract:
Healthcare application is a promising sector for semiconductor industry. Currently, chronic diseases account for over 1/3 of deaths around the world. To mitigate the impact of the diseases, healthcare paradigm is now shifting from reactive illness management towards proactive and preemptive health management; the goal here is to maintain healthy life in the first place, or prevent illness from getting any worse by continuously monitoring health during normal daily life. This tutorial covers two topics of biomedical microsystem design under the umbrella of wearable healthcare. We will begin with circuit design strategy for biomedical sensors. Both analog front-end and digital back-end will be shown with examples. Then we will move on to wearable body area network (WBAN). WBAN is a strong candidate to realizing continuous health monitoring environment. During the course, two types of Wearable BAN (wireless and wired) will be introduced, and their various aspects are thoroughly reviewed. Low energy circuit techniques to overcome their limitations will also be discussed. Finally, several examples of wearable healthcare system implementation will be presented.

Instructor(s):
Jerald Yoo, Assistant Professor,
Masdar Institute, Abu Dhabi, United Arab Emirates.

Jerald Yoo (S’05-M’10) received the B.S., M.S., and Ph.D. degrees in Department of Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2002, 2007, and 2010, respectively. In May 2010, he joined the faculty of Microsystems Engineering, Masdar Institute, Abu Dhabi, United Arab Emirates, where he is an assistant professor. He is currently also with Technology and Development Program, Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, as a research affiliate. He developed low-energy Body Area Network (BAN) transceivers and wearable body sensor network using Planar-Fashionable Circuit Board (P-FCB) for continuous health monitoring system. His research focuses on low energy circuit technology for wearable bio signal sensors, wireless power transmission, SoC design to system realization for wearable healthcare applications, and energy-efficient biomedical circuit techniques. He is an author of a book chapter in Biomedical CMOS ICs (Springer, 2010). Dr. Yoo is a co-recipient of the Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Awards in 2005.
Design Methodology for Robust Clock Networks

Abstract:
This tutorial covers the clock network design methodology, especially focusing on the construction of robust clock under PVT (process-voltage-temperature) variation. First, the basic synthesis flow of clock networks is described with the emphasis of key factors to be considered during the design process. Second, a more in-depth analysis and the related problems caused by the PVT variation are discussed, followed by enumerating the state-of-art design and optimization techniques to address the problems. Thirdly, the diverse structures of clock networks are described, and their pros and cons are summarized with a numeric data extracted from intensive simulation. Finally, the clock design flow is moved to the area of 3D ICs, and what the unique issues to be addressed are and how they are currently solved will be presented.

Instructor(s):
Taewhan Kim, School of Electrical Engineering and Computer Science, Seoul National University, Seoul, South Korea.

Taewhan Kim received the B.S. degree in computer science and statistics and the M.S. degree in computer science from Seoul National University, Seoul, Korea, and the Ph.D. degree in computer science from the University of Illinois at Urbana-Champaign, Urbana, in 1993.

He is currently a Professor with the School of Electrical Engineering and Computer Science, Seoul National University. After graduation, he was with Lattice Semiconductor Corporation and Synopsys, Inc., San Jose, CA, for six years, specializing in design automation tool development. He has published over 160 technical papers in international journals and conferences, including the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, the IEEE Transactions on Very Large Scale Integration, ACM TODAES, DAC, ICCAD, and ASPDAC. His current research interests include computer-aided design of integrated circuits ranging from the architectural synthesis through physical designs, specifically focusing on power, thermal, noise, reliability, and 3-D ID design issues. Dr. Kim is the Editor-in-Chief of the International Journal of Computing Science and Engineering.