Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 422-423

P2-6

A New Approach to Gate Dielectric Integrity Based on Differences Between i) Strained and ii) Strain-free Interfacial Regions: *Applications to Devices with Alternative High-k Gate Dielectrics*

G. Lucovsky[1], J.C. Phillips[2] and P. Boolchand[3]

[1]North Carolina State University, Department of Physics
Campus Box 8202, Raleigh, NC 27965-8202, USA
Phone: +01 919-515-3301 Fax: +01-919-515-7331 E-mail: glucovsky@aol.com
[2] Rutgers University, New Brunswick, NJ, USA
[3]Department of Electrical and Computer Engineering, University of Cincinnati, Cincinnati OH, USA

1. Introduction

It is well established that Si-SiO_2 interfaces in MOSFET devices are not atomically abrupt, but instead contain i) a transition region ~0.5 nm thick in which the distribution of local bonding arrangements have average SiO composition, as well as ii) a strained or *defective* region in the Si substrate that is of similar spatial extent and that likely contains Si dangling bonds [1,2]. Similar interfacial transition regions have been found at interfaces between Si and high-k dielectrics as well. It is therefore critically important to understand i) the basic physical and chemical forces that drive the creation of these regions, ii) the bonding within these regions, and iii) the effects that these regions have on device performance and reliability. This paper addresses these issues by combining new and important insights in the nature of self-organized regions that develop at compositional interfaces between unconstrained and heavily constrained materials; i.e., the Si and SiO_2 of the hetero-interface. Three factors contribute to the formation of these transition regions; i) differences in Si-Si interatomic-distances in the Si substrate and the SiO_2 dielectric result in intrinsic compressive stress in the oxide and tensile stress in the substrate, ii) differences in linear thermal expansion coefficients in the Si and the substrate add a thermally-induced stress component, and iii) differences in the average number of bonds per atom, 4 in the substrate, and 2.7 contribute to bond-strain at the atomic scale. Significant experimental results for Si-SiO_2 interfaces are summarized, and then discussed in the context of physical and chemical bonding mechanisms with an emphasis on gate dielectric interface integrity at a microscopic bonding level that is readily extended to Si-high-k dielectric interfaces.

2. Experimental Results

a) Studies of medium ion energy scattering identified SiO_x and defective Si interfacial regions ~ 0.5 nm thick at Si-SiO_2 interfaces [1].

b) Spectroscopic ellipsometry studies confirmed the SiO_x regions, but did not include defective Si in the modeling analysis [2].

c) A combination of optical second harmonic generation and C-V measurements identified two different transition temperatures, one for Si-SiO_2 interface relaxation at ~900°C, and one for intrinsic growth stress relaxation at ~1000°C [3].

3. Physical Mechanisms for Interface Relaxation

Lucovsky and Phillips and coworkers applied the concepts of constraint theory developed to explain glass formation in chalcogenide and oxide glasses, to Si-dielectric interfaces [4], providing important insights to the physical mechanisms underlying i) the formation of interfacial transition regions, and ii) defect formation and defect relaxation at these interfaces. This approach represents builds on the studies of Boolchand and co-workers on the nature of the glass transition, and the compositional dependence of transitions in a alloy regimes in a glass forming chemical system, e.g., a-$Se_{1-x}Ge_x$, which are associated with a change from compliant or under-constrained bonding in a-Se, to rigid or over-constrained bonding in an alloy with 33% Ge [5]. Lucovsky. Phillips and coworkers pointed out that Si-SiO_2 and Si-Si_3N_4 interfaces were hetero-structures in which in which the substrate Si was rigid or over constrained with the number of bonds/atom equaling exactly four, and the number of valence bonding constraints per atom being greater than the network dimensionality of three. In contrast, these two dielectrics have different numbers of bond/atom, and valence bonding constraints per atom, spanning a range from i) an ideal non-crystalline solid for SiO_2 in which the number of bonding constraints per atom is the same as the network dimensionality, three, to iii) over-constrained or rigid Si_3N_4 dielectric in which the number of bonding constraints per atom is substantially greater than three. In this paper we apply for the first time constraint theory with macroscopic strain, both intrinsic and thermally-generated.

Differences in the Si-Si interatomic distances in Si (0.235 nm) and SiO_2 (~0.305 nm) result in intrinsic interfacial strain, tensile in the Si, and compressive in SiO_2. In addition, differences in linear coefficients of expansion between Si and SiO_2 result in an additive contribution of thermally-induced strain after high temperature processing steps.

The combination of bonding constraint differences at the Si-dielectric interfaces, intrinsic bond-length strain, and thermally-induced strain result in a muli-component interfacial transitions region as pictured in Fig. 1. After a thermal anneal at 900°C, there is i) a region of strained or defective Si in tensile stress in the Si substrate, ii) a self-organized, strain free transition region with suboxide

bonding, and iii) a region in which there is a compressive stain gradient in the stoichiometric dielectric (SiO_2, Si_3N_4, or a Si oxynitride alloy). The strain free region represents a balance between intrinsic and thermally induced tensile stress and bond-strain induced compressive stress. Many of the empirically defined metrics for device scaling are determined by this multi-component interfacial region including the universal mobility curves, and U-shaped variation of d_{it} with energy in the forbidden gap.

4. Interface Integrity

Boolchand and coworkers have shown that glasses outside of a compositional *window* in which self-organized, strain free glasses exist, age irreversibly, whereas, glasses inside the window, do not age at all [6]. In this paper, an analogy is drawn between aging, and current or bias voltages stress induced defect generation, either during device operation on a scale of years, or during accelerated stress testing on a scale of hundreds to thousands of seconds. Applying the glass results to the integrity issues this is consistent with stress bias/current induced defects being generated in the strained Si region of the substrate, or in the bulk of the dielectric, but not in the interfacial SiO_x strain region.

In particular, increases in the densities of interface traps which reduce the transconductance through a shallow trap controlled mobility in the channel region, and stretch out the C-V characteristic producing increases in the threshold voltage are associated with defect formation in the strained Si in contact with the SiO_x region, whereas soft and hard break down events take place in the bulk of the dielectric film. These two regions are not strain free either on a bonding scale, or a macroscopic strain field scale. However, even though the SiO_x region is not optimized with respect to bonding constraints per atom, there is a relief of bond strain induced compressive stress by macroscopic tensile stress associated with bond length induced strain of the Si substrate.

The application of these ideas to high-k dielectrics will be discussed, and involves applying bond constraint counting approaches that are applicable to ionic bonding arrangements in transition metal high-k dielectrics and Al_2O_3 [7]. For example the average number of bonds/atom in Al_2O_3 is 3, corresponding to 4.5 bonding constraints per atom. This increases the effective compress stress in the dielectric, and leads to an increase in tensile stress in the Si substrate increasing the number of density of dangling bond defects by a factor of 4-6 as reported by Stesmans et al.[8].

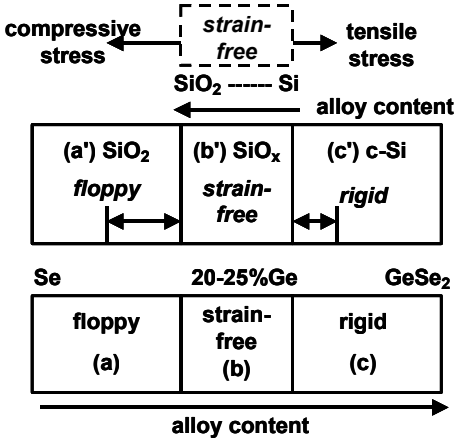
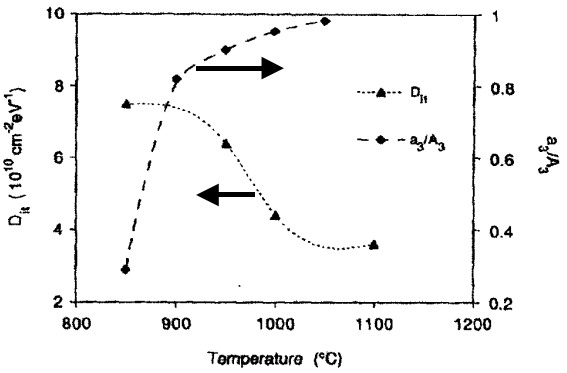


Fig. 1. Schematic of analogy between (a) floppy, (b) in the compositional strain-free, self-organized, and (c) rigid regimes diagram of a non-crystalline binary alloy system (Se-Ge), and the corresponding (a) floppy-SiO_2, (c) strain-free, self-organized SiO_X, and rigid c-Si substrate regions of a gate dielectric interface. The head to tail arrows indicate the stress regions where defect generation occurs.

Fig. 2. D_{it} relaxation is proportional to integrated oxide stress,



whereas interface self-organization, as monitored by optical second harmonic generation occurs at a lower temperature.

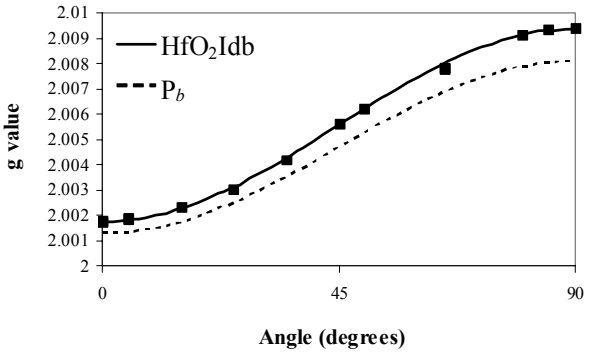


Fig. 3. Angular dependence of g-tensor indicates a 'flatter' dangling bond site at HfO_2 - Si (solid) than at SiO_2-Si interface (dashed). (Lenahan and Conley, private commun.).

References

1. N.W. Cheung et al., Phys. Rev. Lett. **41**, 1396 (1978).
2. D.E.Aspnes et al. Phys. Rev. Lett. **43**, 1046 (1979).
3. C. Bjorkman et a.l, JVST **B11**, 1521, (1993)
4. G. Lucovsky et al., APL, **74**, 2005 (1999).
5. P. Boolchand, in *Insulating and Semiconducting Glasses* (World Scientific, Singapore, 2000), p. 191.
6. S. Chakravarty et al. Phys. Rev. Letters (2003), in press.
7. R. Kerner, J.C. Phillips, SS Commun. **117**, 47 (2000).
8. A. Stesmans, V.V. Afanase'v, JVST **B20**, 1720 (2002).