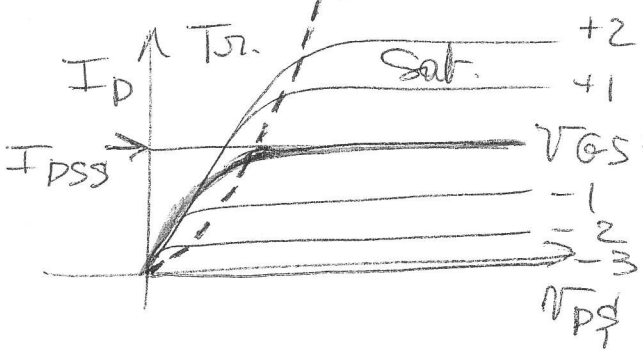
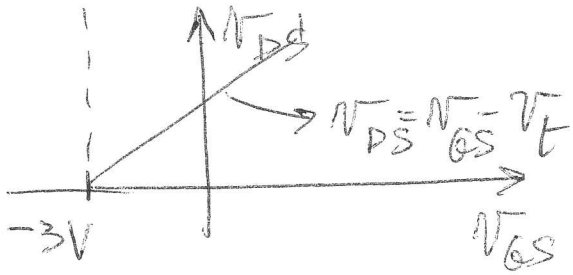
Problem 4.115 p375

A depletion-type n-channel MOSFET with $k_n'\left(\frac{W}{L}\right) = 2\ mA/V^2$ and $V_t = -3V$ has its source and gate grounded. Find the region of operation and the drain current for $v_D = 0.1\ V$, $1\ V$, $3\ V$, and $5\ V$. Assume $\lambda = 0$.





$v_{DS} \leq \underbrace{v_{GS}}_{0} - V_t = 3V$

So for $v_{DS} = v_D < 3V$ Triode mode of operation

for $v_{DS} = v_D > 5V$ Saturation mode

$v_D = 0.1 > 1V$ $\quad I_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_D - \frac{1}{2}v_D^2\right]$

$v_D = 0.1V \rightarrow I_D = 0.59\ mA$

$v_D = 1V \rightarrow I_D = 5\ mA$

for $v_D = 3$ & $5V$ $\quad I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left[v_{GS} - V_t\right]^2$

$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)9 = 9\ mA = I_{DSS}$

Section 4.4 The MOSFET as an amplifier and as a switch.

When operated in saturation, the MOSFET acts as a voltage controlled current source. Changing v_{GS} controls I_D. So, when operated in saturation mode, the MOSFET can be used as a transconductance amplifier (Chapter I).

v_{DS}
$\parallel$
$v_O = v_{DD} - R_D I_D$

$\rightarrow I_D = \dfrac{v_{DD} - v_{DS}}{R_D}$

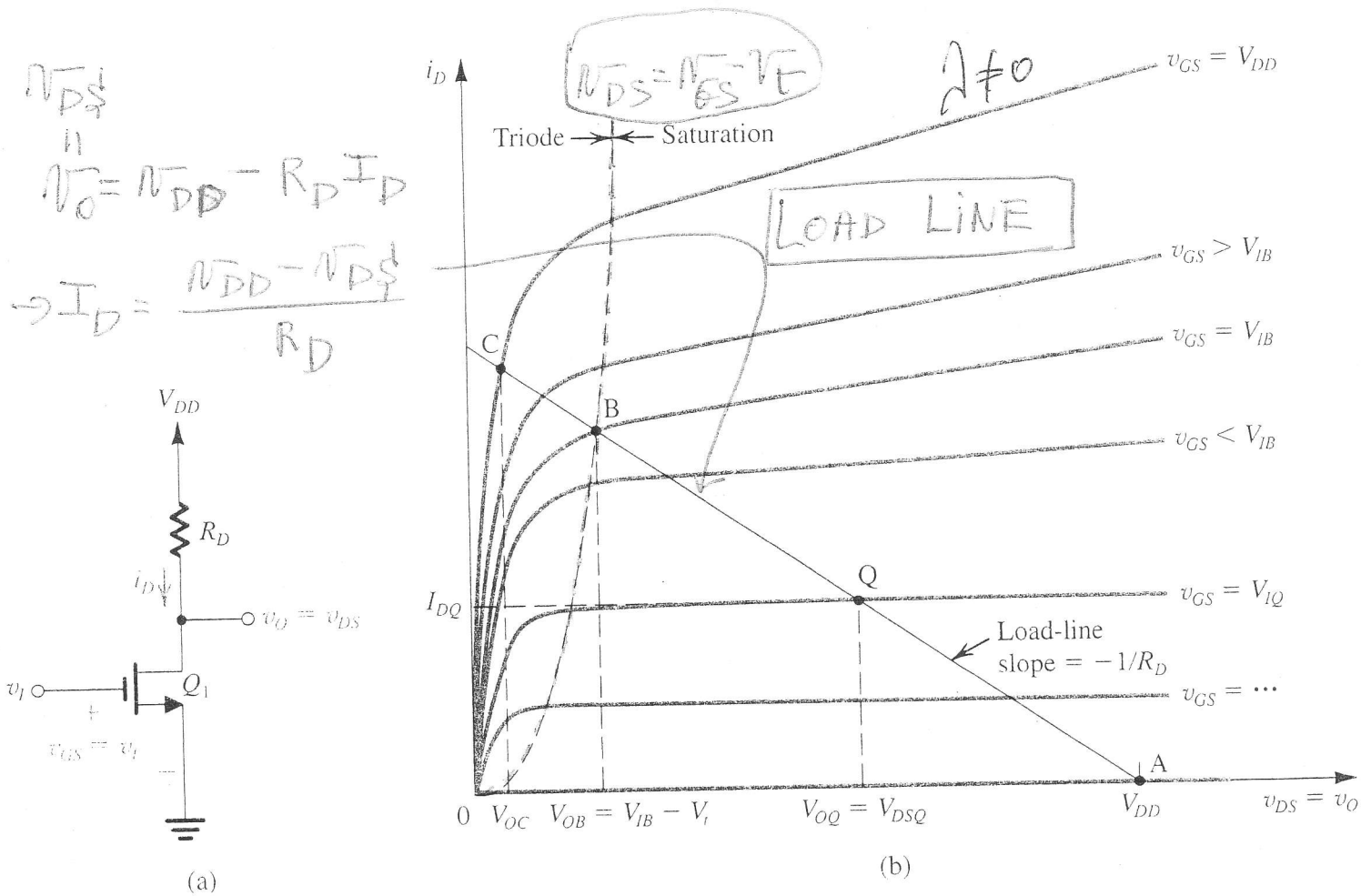
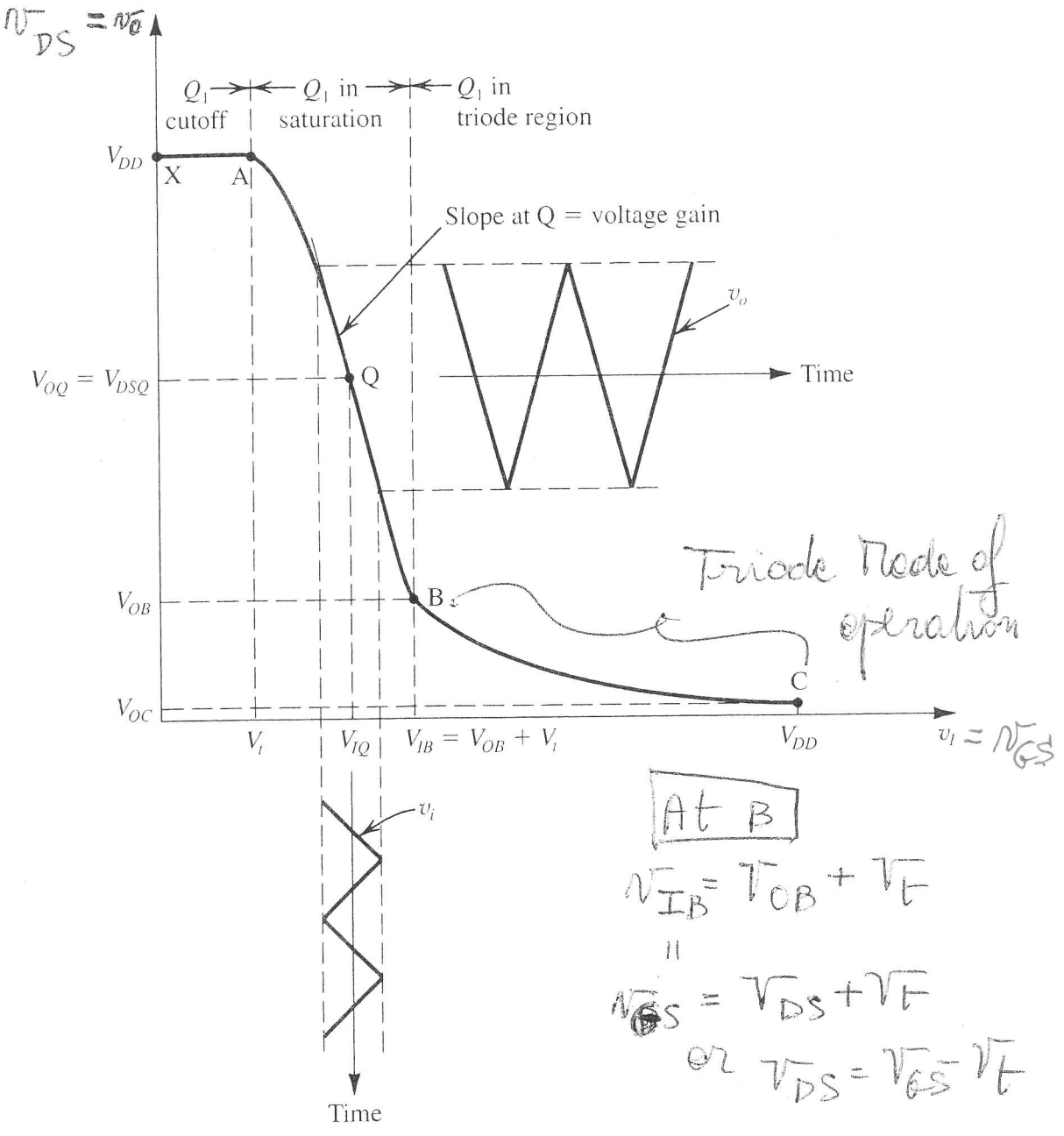


FIGURE 4.26 **(a)** Basic structure of the common-source amplifier. **(b)** Graphical construction to determine the transfer characteristic of the amplifier in (a).

TRANSFER CHARACTERISTIC OF MOSFET



(c)

FIGURE 4.26 *(Continued)* **(c)** Transfer characteristic showing operation as an amplifier biased at point Q.

§4.5 Biasing in MOS Amplifier Circuits pp. 280–286

§4.5.1 Biasing by fixing V_{GS}

$$I_D^{sat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

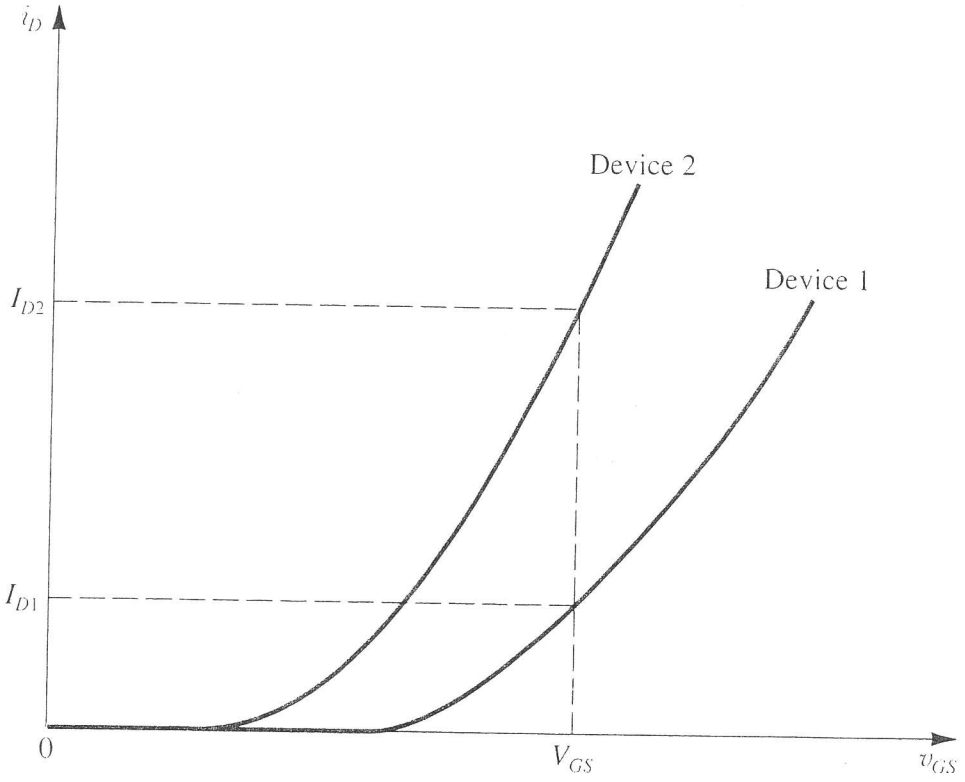


FIGURE 4.29 The use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D. Devices 1 and 2 represent extremes among units of the same type.

$\frac{W}{L}$, μ_n, C_{ox}, V_t can vary from device to device.

For given V_{GS} → many values of I_D possible.

This is not a good way to bias a MOSFET.

§4.5.2 Biasing by Fixing V_G and connecting a resistance in the source.

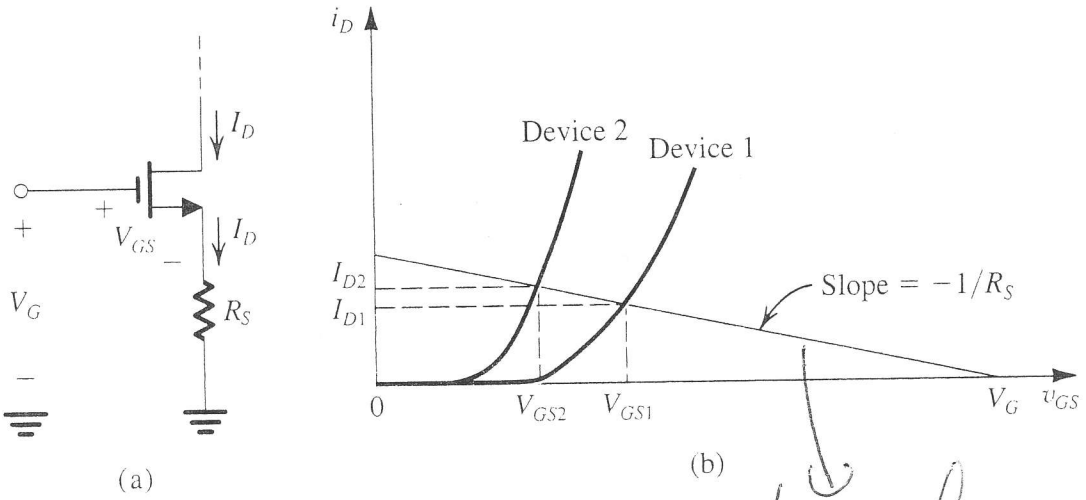


Fig. 4.30

LOAD LINE due to R_S

fixed $\rightarrow V_G = V_{GS} + R_S I_D$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

If $V_G \gg V_{GS}$, I_D does not vary much from device to device.

R_S provides negative feedback

If $I_D \uparrow$ for some reason, since V_G is fixed, V_{GS} has to decrease. Hence I_D will decrease. So R_S helps keeping I_D stable.

STABILITY $\longleftrightarrow$ NEGATIVE FEEDBACK

MORE IN EE352

Practical discrete implementations of biasing scheme

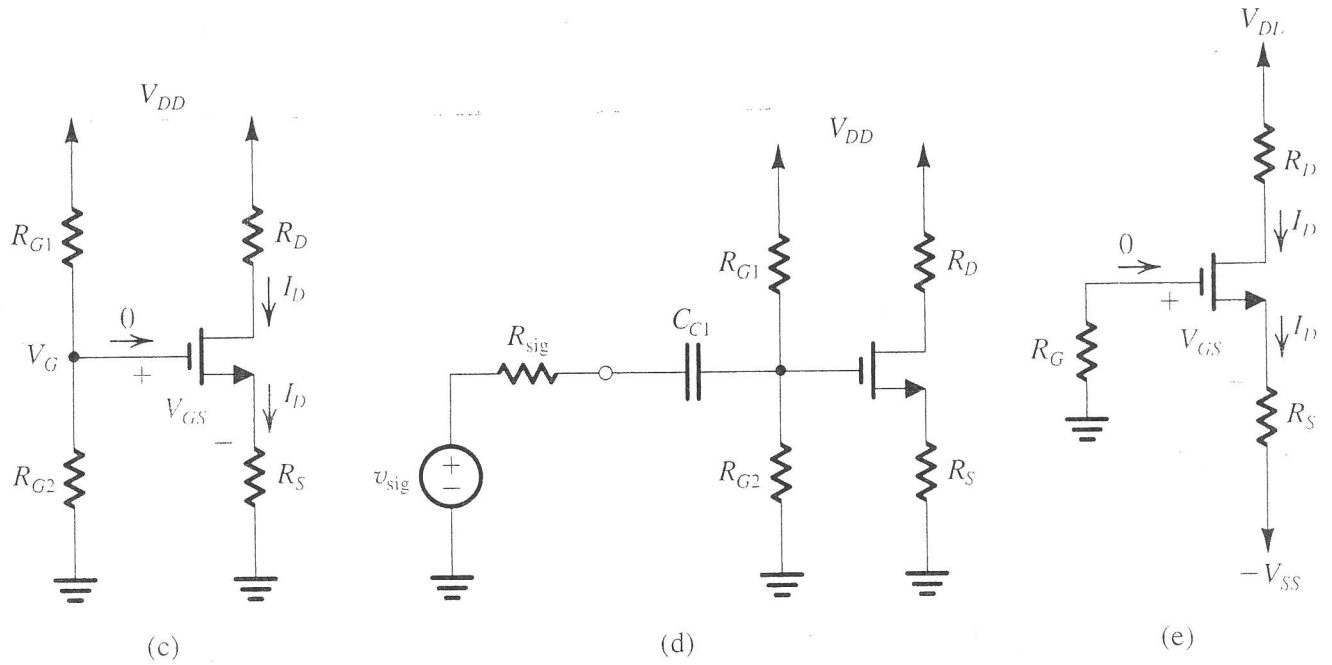


FIGURE 4.30 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(a)** basic arrangement; **(b)** reduced variability in I_D; **(c)** practical implementation using a single supply; **(d)** coupling of a signal source to the gate using a capacitor C_{C1}; **(e)** practical implementation using two supplies.

For amplification, the biasing resistors must be selected so that MOSFET stays in saturation mode of operation.

4.5.3 Biasing Using a Drain-to-Gate feedback resistor

R_G is in MΩ range

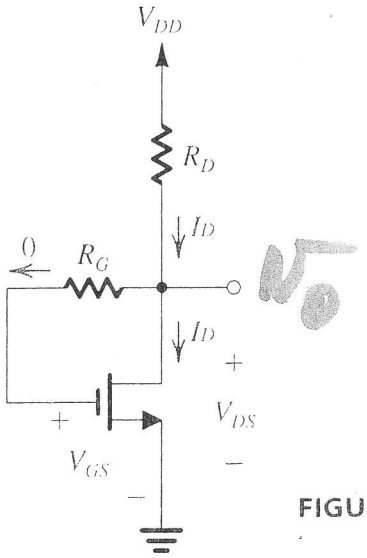


FIGURE 4.32

works also for NMOS, PMOS enhancement and depletion mode.

R_G is the feedback resistor (usually MΩ range)

$I_G = 0 \qquad V_{GS} = V_{DS} = V_{DD} - R_D I_D$

$V_{DD} = V_{GS} + R_D I_D$

As before, if I_D increases for some reason, V_{GS} must decrease since V_{DD} is fixed. Hence, I_D decreases, a change opposite to the one originally assumed. In other words, I_D stays stable.

The NEGATIVE feedback of R_G works to keep the value of I_D as constant as possible.

STABILITY ⟷ NEGATIVE FEEDBACK

MORE IN EE352

4.5.4 Biasing Using a constant current source (p. 286)

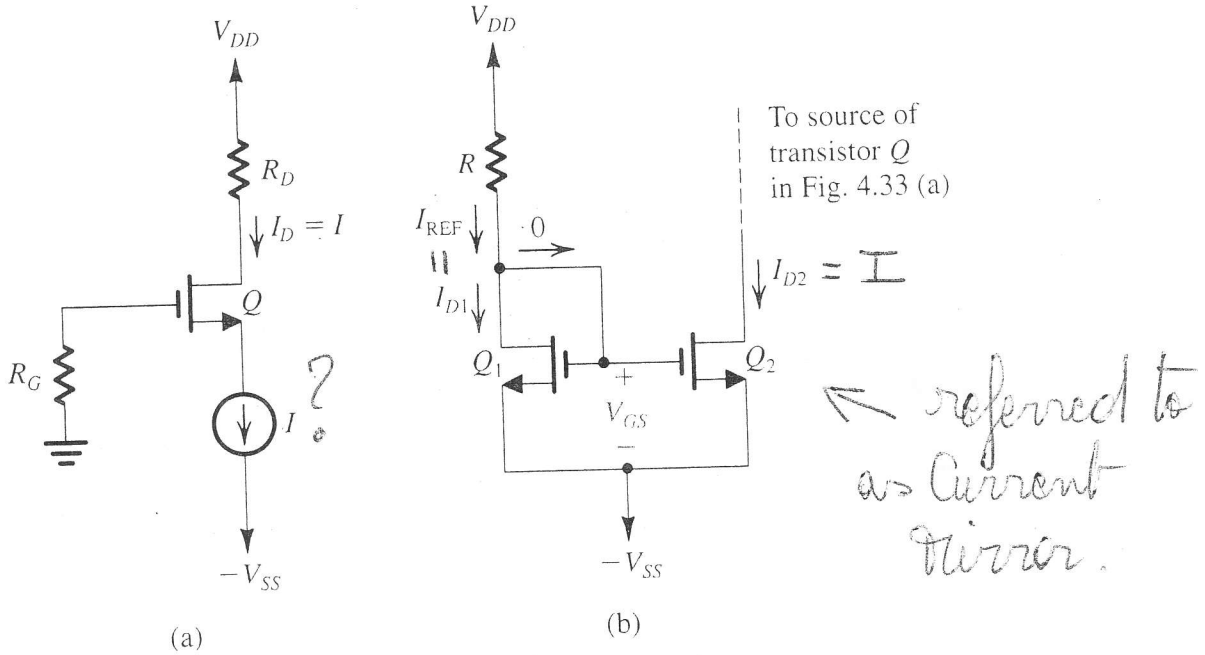


FIGURE 4.33 **(a)** Biasing the MOSFET using a constant-current source I. **(b)** Implementation of the constant-current source I using a current mirror.

Implementation of constant current source I and concept of current mirror.

Q_1 has its drain shorted to its gate → It is automatically in saturation mode. I_D of Q_1 is supplied by V_{DD} through resistor R.

Gate currents are ZERO

Hence

$$I_{D1} = I_{REF} = \frac{V_{DD} + V_{SS} - V_{GS}}{R} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$$

↳ reference current.

Q_2 has same V_{GS} as Q_1. If Q_2 in saturation

$$I_{D2} = I\,(\text{desired value of current source}) = \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2 \rightarrow$$

$$\boxed{I = I_{REF} \times \frac{(W/L)_2}{(W/L)_1}}$$

§4.6 Small Signal operation and models.

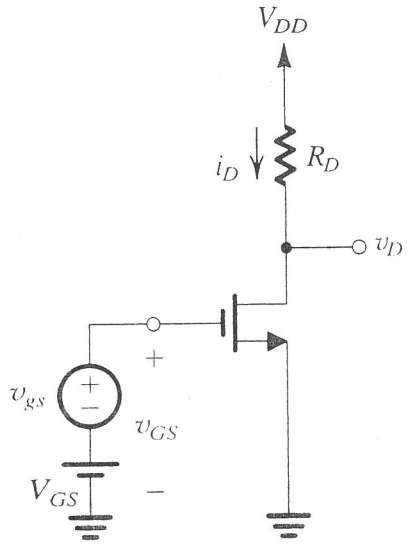


FIGURE 4.34 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

DC Bias Point

$$I_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$V_D = V_{DS} = V_{DD} - R_D I_D \quad \text{(load line)}.$$

For saturation $V_{DS} \geq V_{GS} - V_t$

The signal current in the drain terminal.

Total = DC + AC

$$v_{GS} = V_{GS} + v_{gs}$$

→ instantaneous current i_D

$$i_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} + v_{gs} - V_t)^2$$

$$= \underbrace{\frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2}_{I_D} + \underbrace{k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)v_{gs}}_{i_d = g_m v_{gs}} + \underbrace{\frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{gs}^2}_{\text{negligible if } v_{gs} \text{ small}}$$

Third term negligible if

$$\frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{gs}^2 \ll k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)v_{gs}$$

or

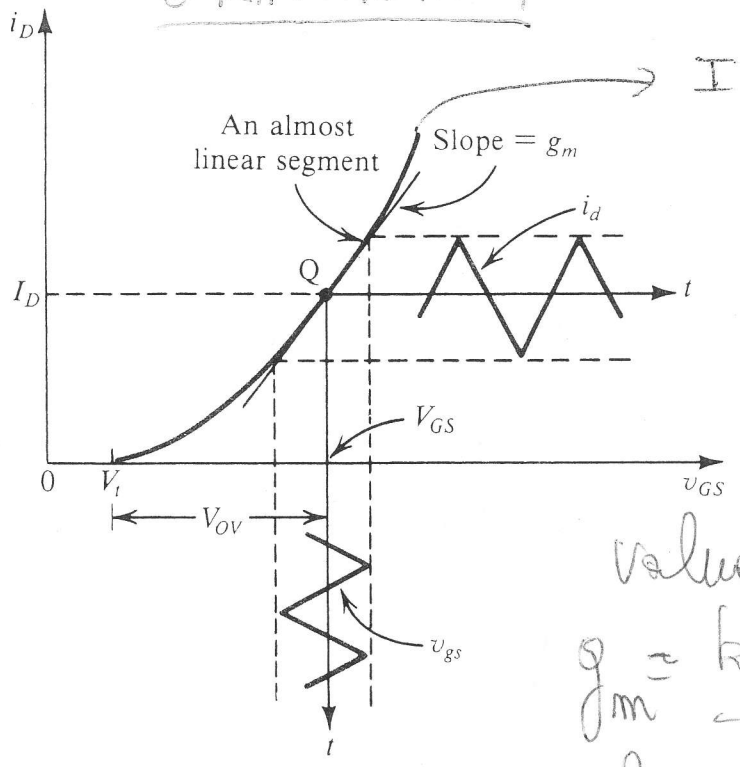
$$v_{gs} \ll 2(V_{GS}-V_t) = 2V_{OV}$$

where V_{OV} is the overdrive voltage.

$$g_m \triangleq \frac{i_d}{v_{gs}} = k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)$$

or $\boxed{g_m = k_n'\left(\frac{W}{L}\right)V_{OV}}$ ← from DC analysis.

GRAPHICALLY



Value?

$$g_m = \underbrace{k'\frac{W}{L}}_{\text{few mA/V}^2}\underbrace{(V_{GS}-V_t)}_{\text{few volts}}$$

$g_m \sim$ 1–10 mS

§4.6.3 The Voltage Gain

$$v_D = V_{DD} - R_D i_D$$

$$= V_{DD} - R_D(I_D + i_d)$$

$$= \underbrace{V_{DD} - R_D I_D}_{V_D} \underbrace{- R_D i_d}_{v_d}$$

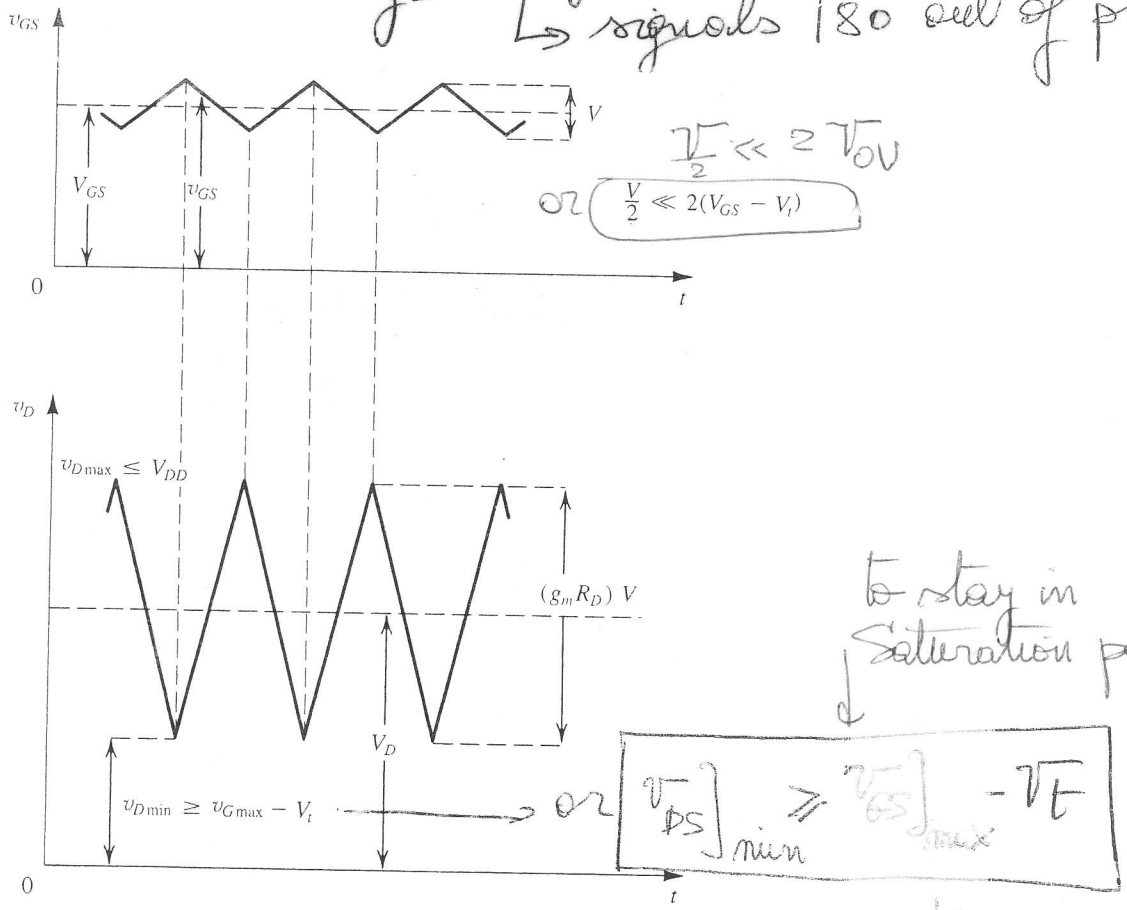
← AC component

So v_d (signal at drain) $= -R_D i_d$

$$v_d = (-g_m R_D) v_{gs}$$

$$A_v = \frac{v_d}{v_{gs}} = -g_m R_D$$

↳ signals 180° out of phase



$\frac{V}{2} \ll 2V_{OV}$

or $\left(\frac{V}{2} \ll 2(V_{GS} - V_t)\right)$

to stay in saturation portion

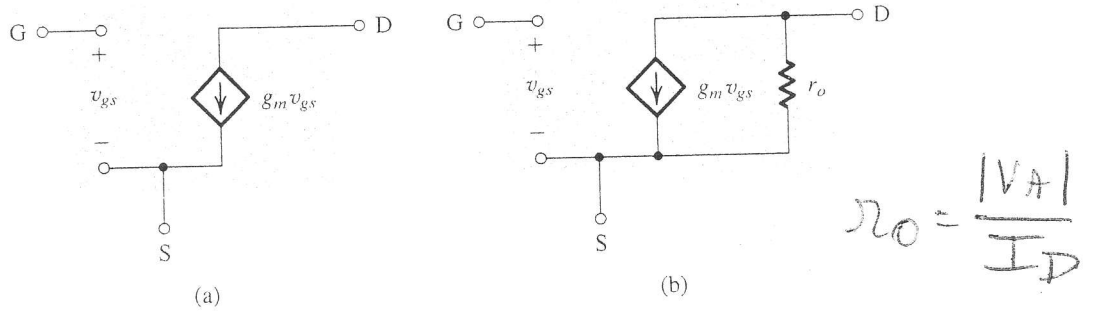
$$v_{DS}\Big]_{min} \ge v_{GS}\Big]_{max} - V_t$$

FIGURE 4.36 Total instantaneous voltages v_{GS} and v_D for the circuit in Fig. 4.34. p. 186 notes

§4.6.5 Small-signal Equivalent Circuit Models

PP. 290 → 296

HYBRID-π model for MOSFET



$$r_o = \frac{|V_A|}{I_D}$$

FIGURE 4.37 Small-signal models for the MOSFET: **(a)** neglecting the dependence of i_D on v_{DS} in saturation (the channel-length modulation effect); and **(b)** including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A|/I_D$.

In analogy with what we saw for BJT, we have the small-signal model for the MOSFET shown above.

The differences are

(1) There is no r_π. The resistance to AC signal between Gate and Source is infinity!

(2) $g_m = k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)$ or $k_n'\left(\frac{W}{L}\right)V_{OV}$

where $V_{OV} = V_{GS} - V_t$ is the overdrive voltage

(3) $r_o = \frac{|V_A|}{I_D}$; $|V_A| = \frac{1}{\lambda}$ where λ = channel length modulation parameter

(4) $I_D^{sat} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{OV})^2 = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \cdot [1 + \lambda V_{DS}]$

usually neglected in DC analysis

Example 4.10 p. 293

Common Source Configuration.

$V_t = 1.5V$

$k_n'\left(\frac{W}{L}\right) = 0.25\ mA/V^2$

$V_A = 50V$

Determine (a) its small-signal voltage gain
(b) its input resistance
(c) The largest allowable input signal.

Neglect effect of r_o in calculating the DC value of I_D

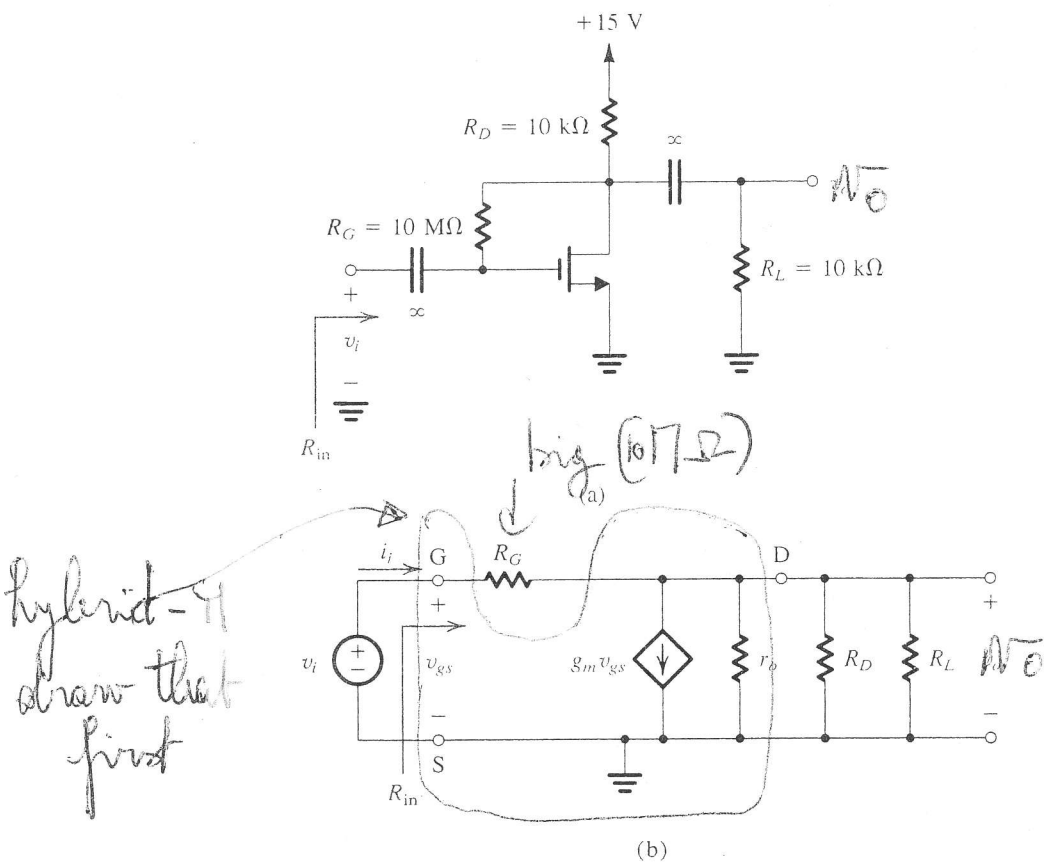


FIGURE 4.38 Example 4.10: (**a**) amplifier circuit; (**b**) equivalent-circuit model.

$$I_D = \frac{1}{2}\,0.25\,(V_{GS}-1.5)^2$$

$V_{GS} = V_D$ because $I_G = 0$

$$\Rightarrow I_D = 0.125\,(V_D - 1.5)^2$$

But $V_D = 15 - R_D I_D = 15 - 10 I_D$ $\Bigg\}$ $\rightarrow I_D = 1.06\,mA$, $V_D = 4.4V$

[The other solution is not physically meaningful.]

$$g_m = k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t) = 0.25\,(4.4-1.5) = 0.725\,mA/V$$

$$r_o = \frac{V_A}{I_D} = \frac{50}{1.06} = \underline{47\,k\Omega}$$

AC analysis

R_G very large. We neglect the current through it.

Hence, $v_o \simeq -g_m v_{gs}(R_D \,//\, R_L \,//\, r_o) = -0.725\,(10\,//\,10\,//\,47)\,v_{gs}$

$v_o / v_{gs} = -3.3\,V/V$

Rin? $\quad i_i = (v_i - v_o)/R_G = \frac{v_i}{R_G}\left(1 - \frac{v_o}{v_i}\right) = \frac{4.3\,v_i}{R_G}$

$$\frac{v_i}{i_i} \triangleq R_{in} = \frac{R_G}{4.3} = 2.33\,M\Omega$$

Largest allowable input signal? We must keep MOSFET in saturation

$$v_{DS} \geq v_{GS} - V_t$$

$$v_{DS,min} = v_{GS,max} - V_t$$

$$V_{DS} - |A_v|\hat{v}_i = V_{GS} + \hat{v}_i - V_t$$

$$4.4 - 3.3\hat{v}_i = 4.4 + \hat{v}_i - 1.5$$

$$\Rightarrow \underline{\hat{v}_i = 0.34\,V}$$

[In negative direction $V_{GS,min}$ $4.4 - 0.34$

$V_{GS,min} = 4.06 > V_t$]

8.4.6.7 The Tequivalent-Circuit Model p. 295

Start with Hybrid-π model

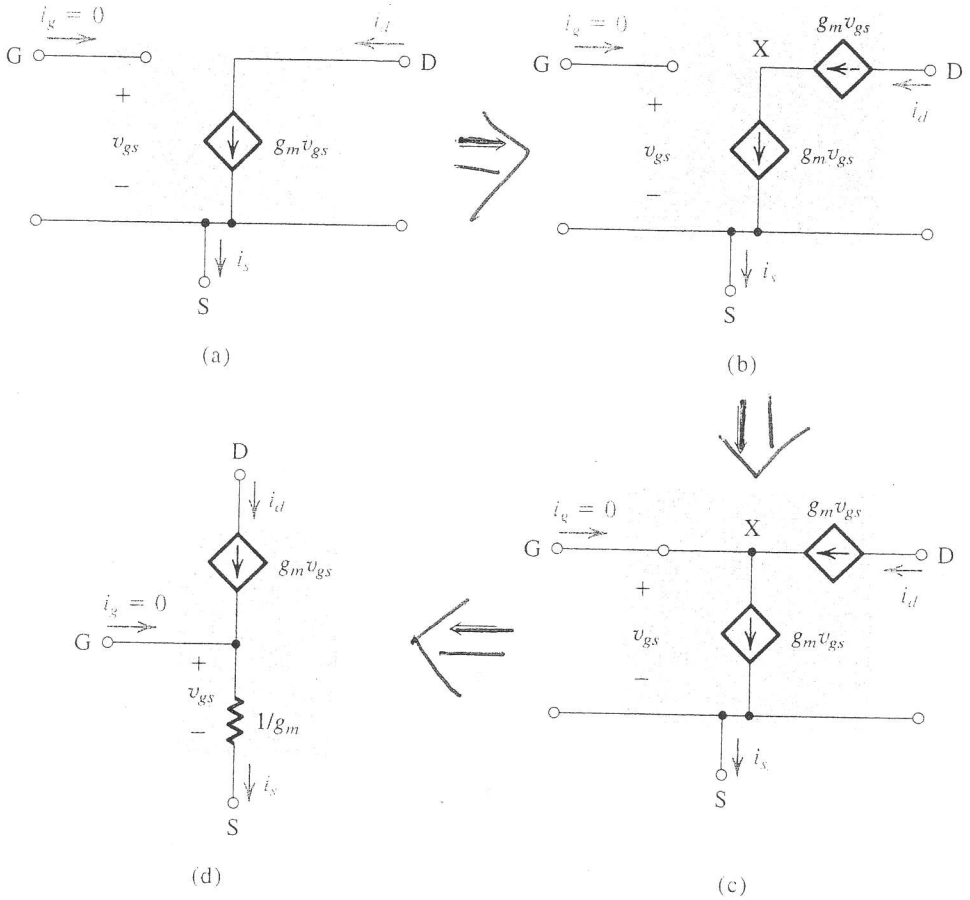
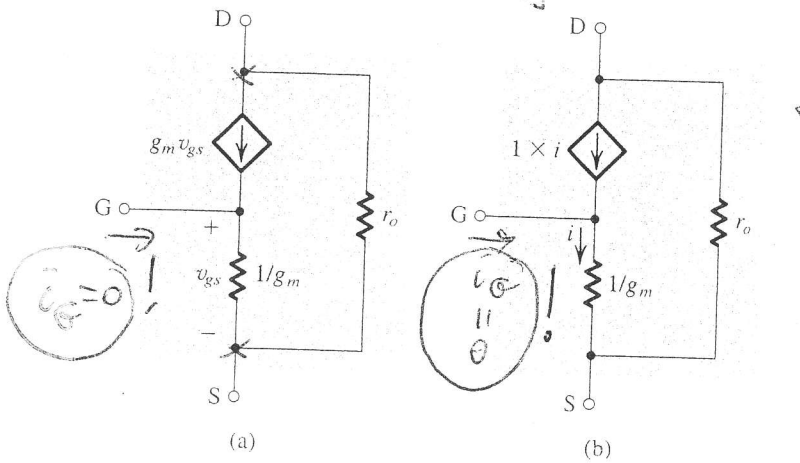


FIGURE 4.39 Development of the T equivalent-circuit model for the MOSFET. For simplicity, r_o has been omitted but can be added between D and S in the T model of (**d**).

Effects of r_o



← looks similar to T-model for BJT, except that $i_G = 0$!

FIGURE 4.40 (**a**) The T model of the MOSFET augmented with the drain-to-source resistance r_o. (**b**) An alternative representation of the T model.

§ 4.7.3 The Common Source amplifier

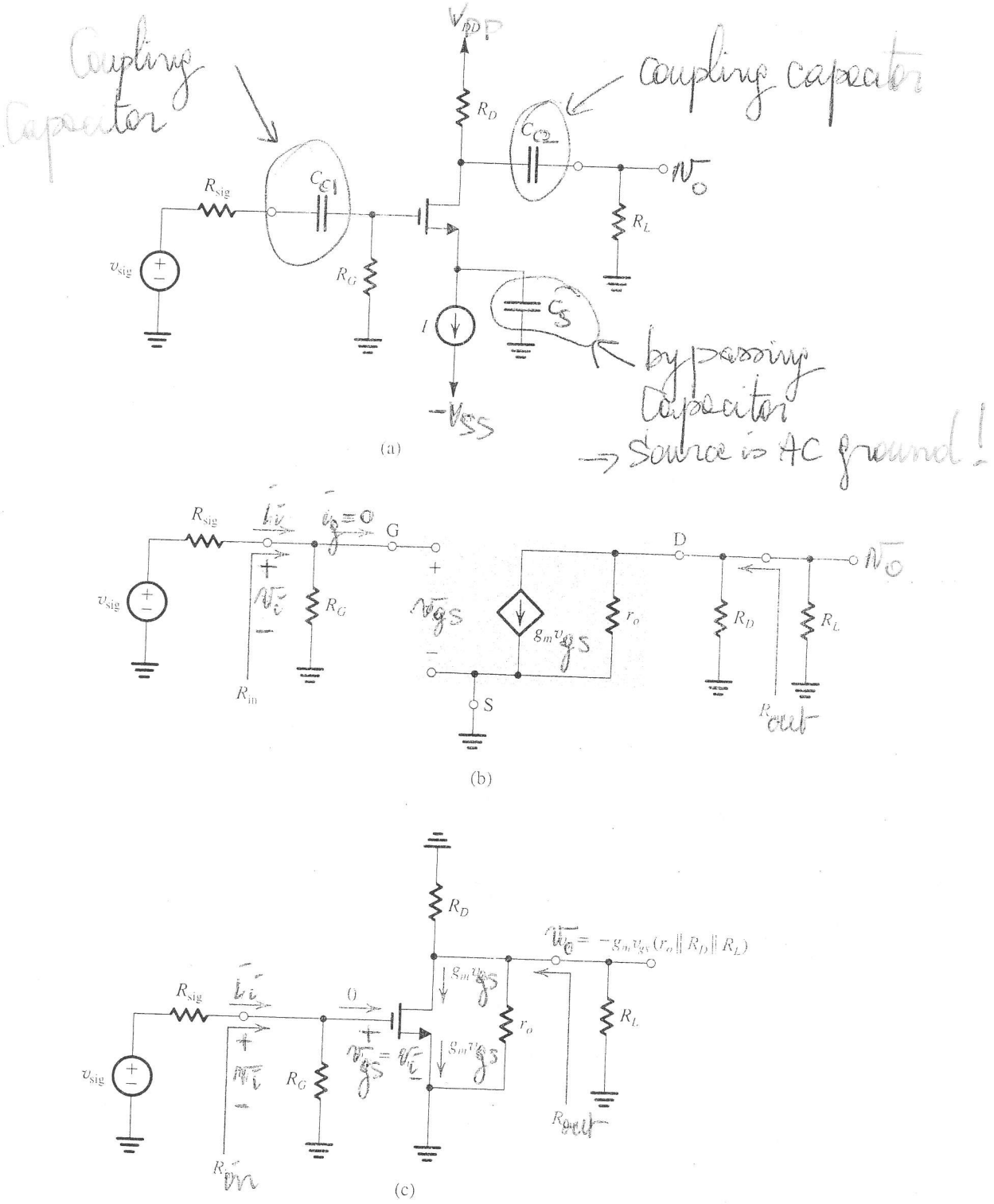


FIGURE 4.43 (a) Common-source amplifier based on the circuit of Fig. 4.42. (b) Equivalent circuit of the amplifier for small-signal analysis. (c) Small-signal analysis performed directly on the amplifier circuit with the MOSFET model implicitly utilized.

$R_{in} = R_G$

so $V_i = V_{sig}\left(\frac{R_{in}}{R_{in}+R_{sig}}\right) = V_{sig}\left(\frac{R_G}{R_G+R_{sig}}\right)$

R_G is usually very large (MΩ range)

So $V_i \approx V_{sig} = V_{gs}$

$$V_o = -g_m V_{gs}(r_o \,//\, R_D \,//\, R_L)$$

$\Rightarrow$ voltage gain $A_v = \frac{V_o}{V_{sig}} = \frac{V_o}{V_{gs}} \cdot \frac{V_{gs}}{V_{sig}}$

So $A_v = -g_m (r_o \,//\, R_D \,//\, R_L) \cdot \left(\frac{R_{in}}{R_{in}+R_{sig}}\right)$

LARGE

R_{out}?

Set $V_{sig} = 0$

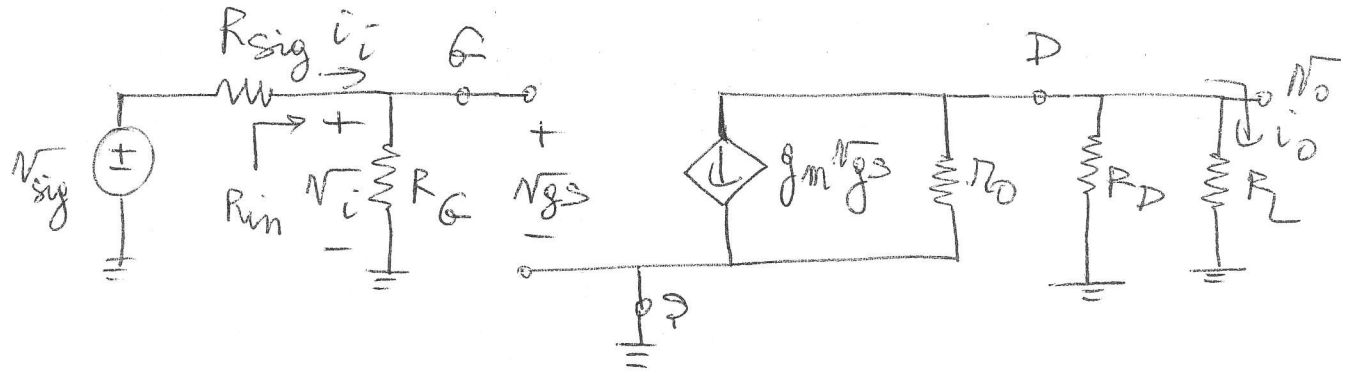
Look back into output terminal.

$\Rightarrow \boxed{R_{out} = r_o \,//\, R_D}$

Typically $r_o > R_D$

Common Source Amplifier

Current gain?



$$i_i = \frac{v_{sig}}{R_{sig} + R_G} \quad ; \quad v_{gs} = \left(\frac{R_G}{R_G + R_{sig}}\right) v_{sig}$$

$$v_o = -g_m v_{gs} \left(r_o // R_D // R_L\right)$$

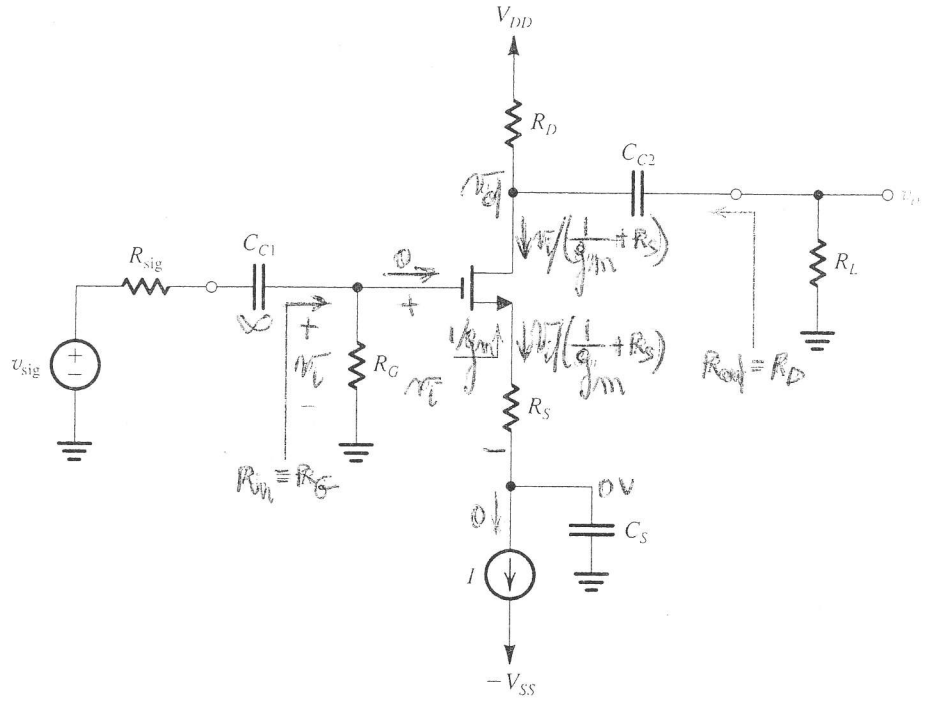
$$i_o = \frac{v_o}{R_L}$$

$$\rightarrow \quad i_o = -g_m \frac{(r_o // R_D // R_L)}{R_L} \left(\frac{R_G}{R_G + R_{sig}}\right) v_{sig}$$

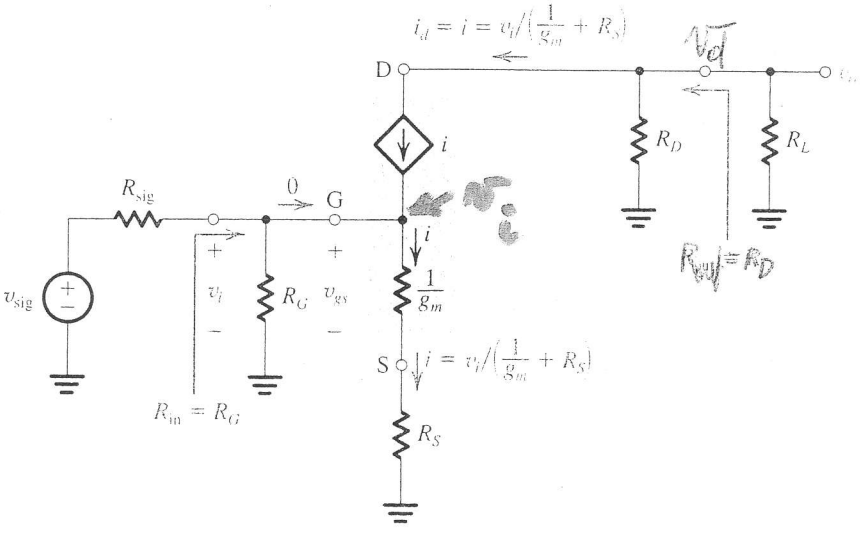
$$i_o = \left[-g_m \left(\frac{R_G}{R_L}\right)\left(r_o // R_D // R_L\right)\right] i_i$$

$$\boxed{\frac{i_o}{i_i} = \left[-g_m \left(r_o // R_D // R_L\right)\right] \left(\frac{R_G}{R_L}\right)}$$

§4.7.4 The Common-Source Amplifier with a Source Resistance



(a)



(b)

FIGURE 4.44 **(a)** Common-source amplifier with a resistance R_S in the source lead. **(b)** Small-signal equivalent circuit with r_o neglected.

$$R_{in} = R_i = R_G$$

$$\Rightarrow \bar{V}_i = \bar{V}_{sig}\left(\frac{R_G}{R_G + R_{sig}}\right)$$

① $\bar{V}_{gs}$ is only a fraction of $\bar{V}_i$. We have a voltage divider with $1/g_m$ and R_S'

$$\bar{V}_{gs} = \bar{V}_i \frac{1/g_m}{\left[1/g_m + R_S'\right]} = \bar{V}_i \Big/ \left[1 + g_m R_S'\right]$$

Because $i_g = 0$, $\bar{I}_d = \bar{I} = \dfrac{\bar{V}_i}{\left[\frac{1}{g_m} + R_S'\right]} = \dfrac{g_m \bar{V}_i}{\left[1 + g_m R_S'\right]}$

It is as if $g_m \longrightarrow \dfrac{g_m}{1 + g_m R_S'}$

↑ see before when $R_S = 0$.

Output voltage $\quad \bar{V}_o = -\bar{I}_d (R_D /\!/ R_L)$

So $\bar{V}_o = \underbrace{\left\{\dfrac{-g_m (R_D /\!/ R_L)}{1 + g_m R_S'}\right\}}_{A_V \triangleq \text{voltage gain}} \bar{V}_i$

Overall voltage gain

$$\boxed{\frac{\bar{V}_o}{\bar{V}_{sig}} = \left(\frac{\bar{V}_o}{\bar{V}_i}\right)\left(\frac{\bar{V}_i}{\bar{V}_{sig}}\right) = -\left(\frac{R_G}{R_G + R_{sig}}\right)\left(\frac{g_m (R_D /\!/ R_L)}{1 + g_m R_S'}\right)}$$

§ 4.7.5 Common Gate Amplifier [p. 311 →]

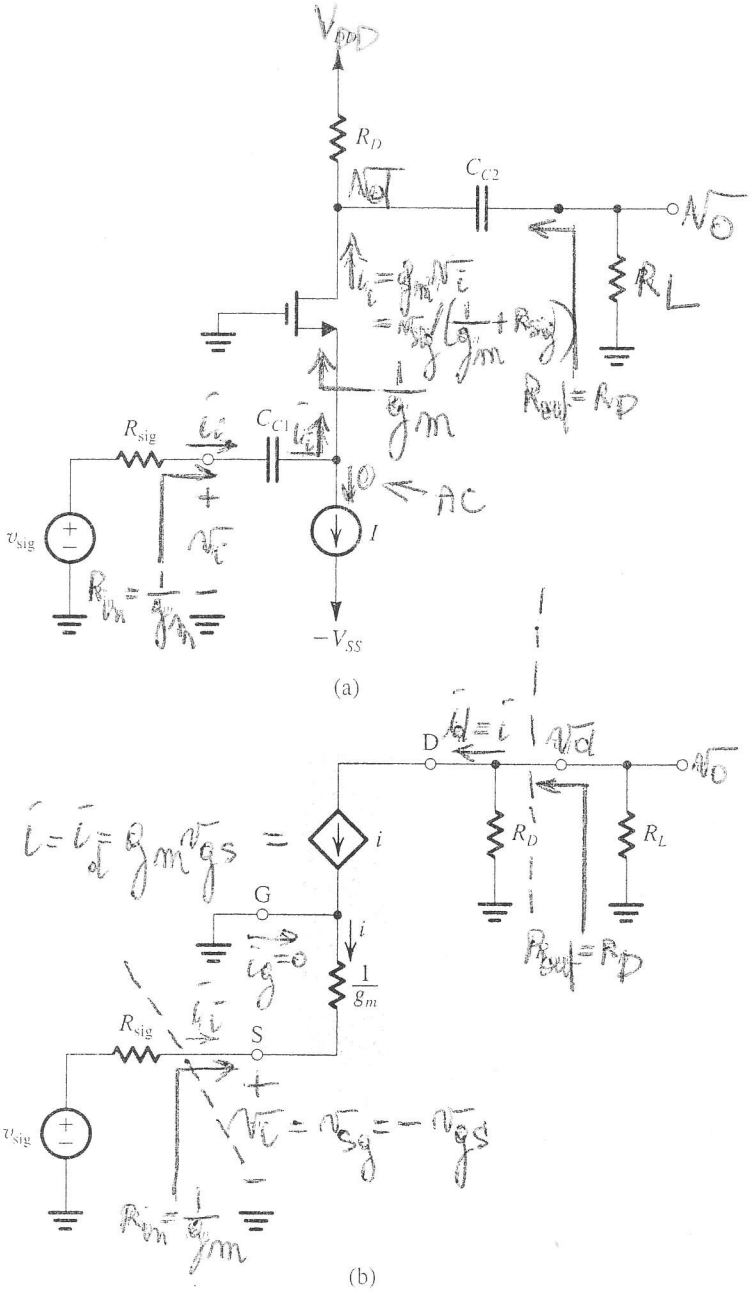


FIGURE 4.43 **(a)** A common-gate amplifier based on the circuit of Fig. 4.42. **(b)** A small-signal equivalent circuit of the amplifier in (a).

$R_{in} = \frac{1}{g_m}$ See Bottom Fig. of previous page.

$g_m \simeq 1\,mA/V \rightarrow R_{in}$ low ($\simeq 1k\Omega$)

→ Voltage is billed at input because R_{in} is low

$$v_i = v_{sig}\left(\frac{R_{in}}{R_{in} + R_{sig}}\right)$$

R_{in} was much larger for Common-Source configuration

$$v_i = v_{sig}\frac{\frac{1}{g_m}}{\left[\frac{1}{g_m} + R_{sig}\right]}$$

$$v_i = \frac{v_{sig}}{\left[1 + g_m R_{sig}\right]}$$

So for $v_i \simeq v_{sig}$ we must select $R_{sig} << \frac{1}{g_m}$

$$i_i = \frac{v_i}{R_{in}} = \frac{v_i}{1/g_m} = g_m v_i$$

$$i_d = \boxed{i = -i_i} = -g_m v_i$$

$$\Rightarrow v_o = v_d = -i_d(R_D // R_L) = g_m(R_D // R_L)v_i$$

So $\boxed{v_o / v_i = +g_m(R_D // R_L)}$ gain has + sign

Overall voltage gain

$$\frac{v_o}{v_{sig}} = \frac{v_o}{v_i} \cdot \frac{v_i}{v_{sig}} = \frac{+g_m(R_D /\!/ R_L)}{1 + g_m R'_{sig}}$$

(non-inverting)

(like for CB for BJTs)

Large

Output resistance

$$\boxed{R_{out} = R_D}$$

Current gain? p.174

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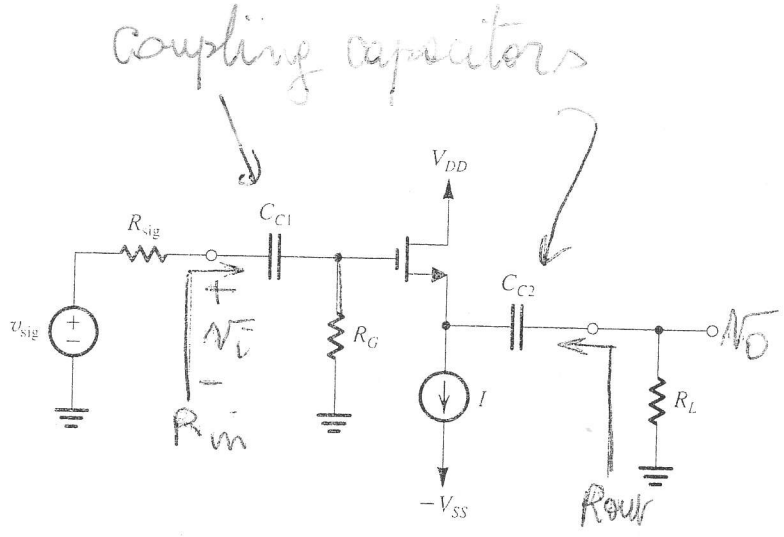
§ 4.7.6 Common Drain

also called [Source Follower] Amplifier p.315.



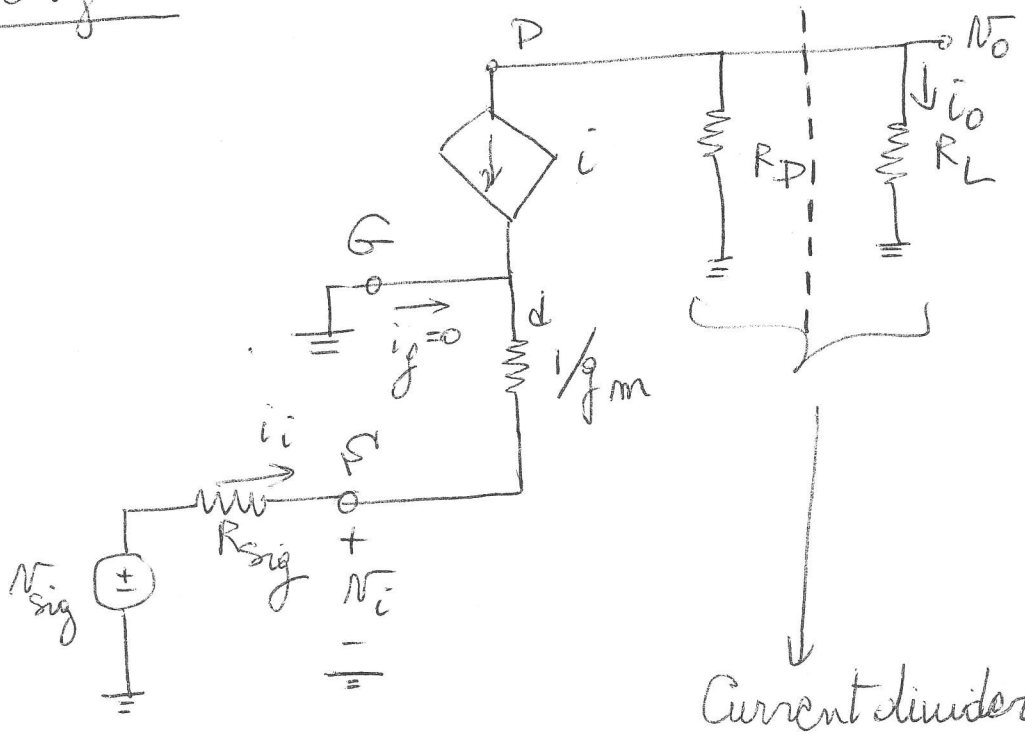
(a)

[Signal on gate, output at Source] "COMMON DRAIN CONFIGURATION"

Fig. 4.46 (a)

Common gate configuration

Current gain



Current divider

$$i_o = \frac{-R_D}{R_D + R_L} \cdot i$$

$$i = -i_i$$

$$\frac{i_o}{i_i} = ?$$

Hence

$$\boxed{\frac{i_o}{i_i} = \frac{R_D}{R_D + R_L} \quad < 1}$$

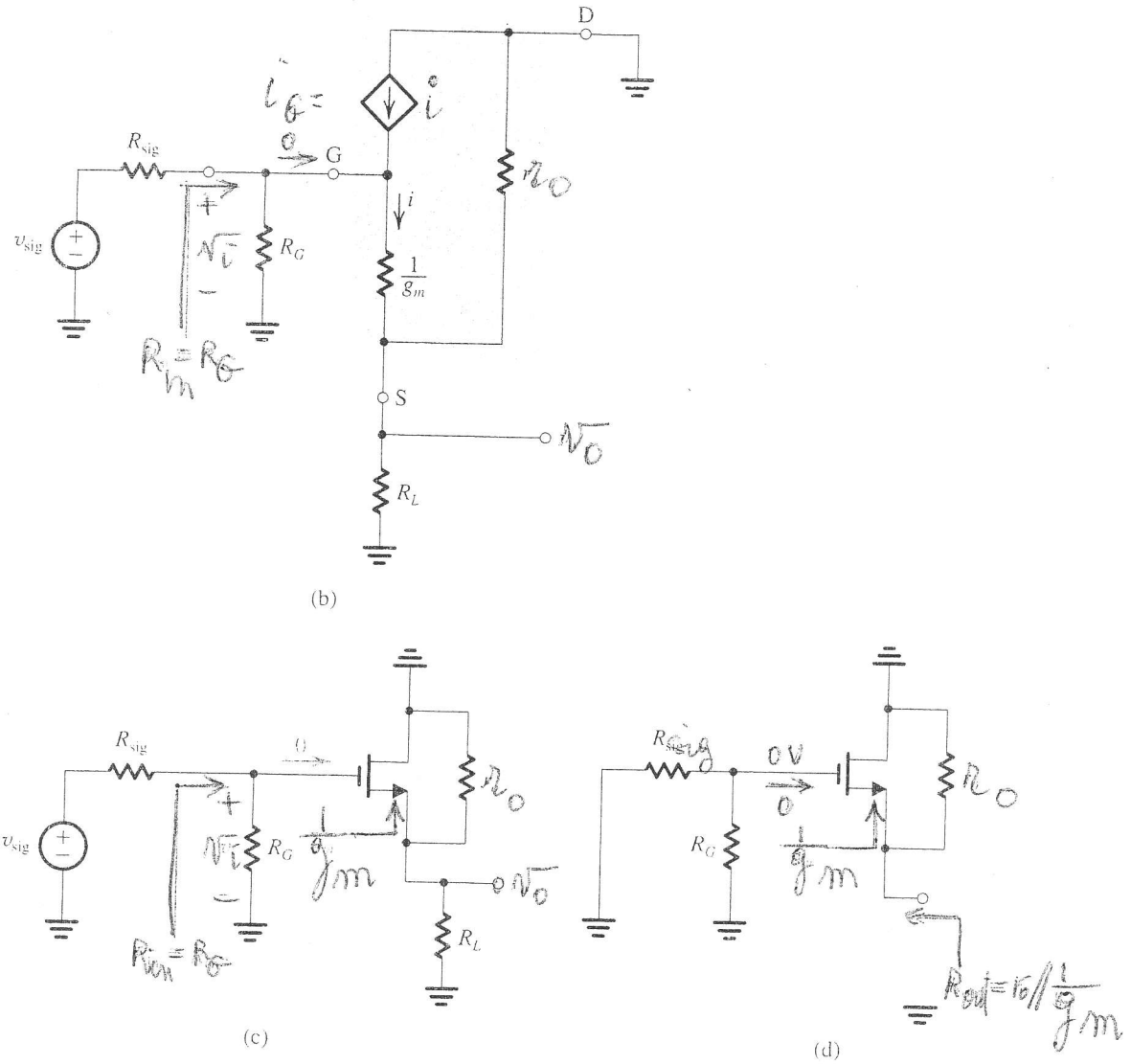


FIGURE 4.46 **(a)** A common-drain or source-follower amplifier. **(b)** Small-signal equivalent-circuit model. **(c)** Small-signal analysis performed directly on the circuit. **(d)** Circuit for determining the output resistance R_{out} of the source follower.

$R_{in} = R_G$ from 4.45(a)

Thus $v_i = v_{sig} \dfrac{R_G}{R_G + R_{sig}} \approx v_{sig}$ if $R_G >> R_{sig}$

r_o is in fact in parallel with R_L.

$\Rightarrow \dfrac{1}{g_m}$ is in series with $(r_o // R_L)$

$$V_o = V_i \frac{(R_L \| r_o)}{\left[(R_L \| r_o) + \frac{1}{g_m}\right]}$$

$$\rightarrow \frac{V_o}{V_i} = \frac{(R_L \| r_o)}{\left[(R_L \| r_o) + \frac{1}{g_m}\right]} \Rightarrow \frac{V_o}{V_{sig}} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_{sig}}$$

↑ close to unity

V_o "follows" (read "is nearly equal to") the voltage at the gate. This is why this configuration is also referred to as "Source follower" or "Unity Gain Buffer Amplifier".

So the overall voltage gain of that configuration is close to unity (as was the common collector configuration for BJTs we studied earlier).

R_{out}? See Fig. 4.46(d)

The gate voltage is zero when we set $V_{sig} = 0$.

looking into source $R_{out} = \left(\frac{1}{g_m} \| r_o\right) \simeq \frac{1}{g_m}$

($\frac{1}{g_m}$: small; r_o: big)

R_{out} ≈ few kΩ (moderately high)

Chapter 4
MOSFETs

Triode Mode $I_D = k_n'\left(\frac{W}{L}\right)\left[(V_{GS}-V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$

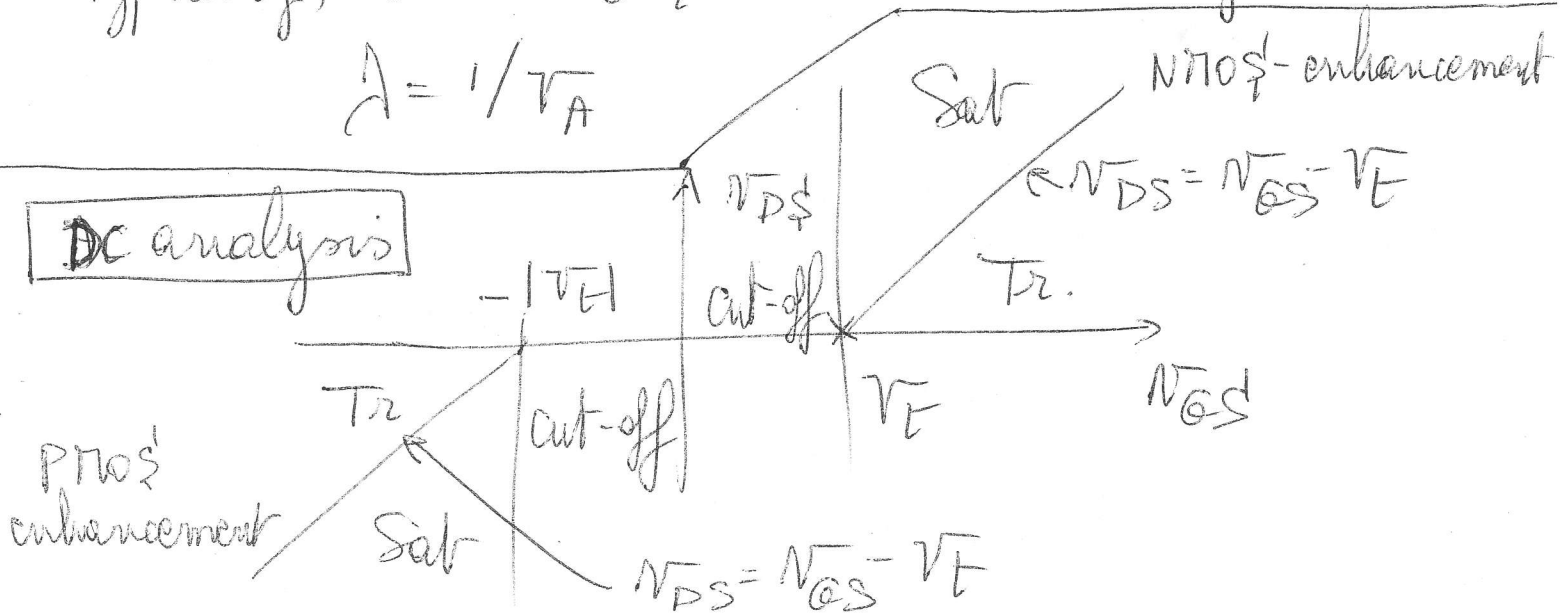
$n \to p$ for PMOS

Saturation Mode $I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)[V_{GS}-V_t]^2(1+\lambda V_{DS})$

Typically, we assume $\lambda = 0$ in DC analysis.

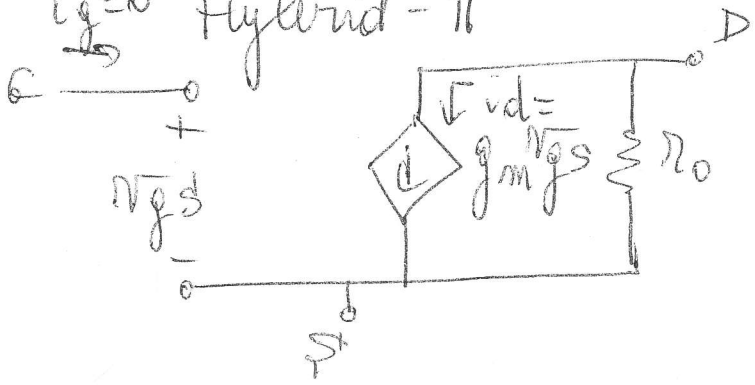
$\lambda = 1/V_A$

DC analysis

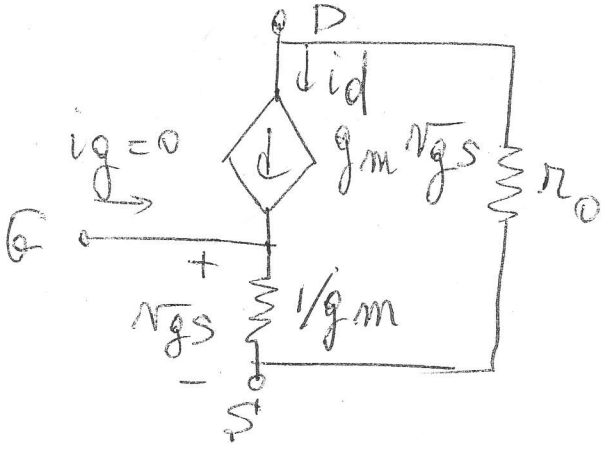


AC analysis

Hybrid-π



T-Model



$g_m = k_n'\frac{W}{L}(V_{GS}-V_t)$

$r_o = \frac{V_A}{I_D}$; $r_o = \infty$ if neglected