A 0.18-μm fabrication process is specified to have $t_{ox} = 4$ nm, $\mu_n = 450$ cm$^2$/V·s, and $V_t = 0.5$ V. Find the value of the process transconductance parameter $k'_n$. For a MOSFET with minimum length fabricated in this process, find the required value of $W$ so that the device exhibits a channel resistance $r_{DS}$ of 1 kΩ at $v_{GS} = 1$ V.

Ans. 388 μA/V²; 0.93 μm

**Ex: 5.1**

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{34.5 \text{ pF/m}}{4 \text{ nm}} = 8.625 \text{ fF/(μm)$^2$}$$

$$\mu_n = 450 \text{ cm}^2/\text{VS}$$

$$k'_n = \mu_n C_{ox} = 388 \text{ μA/V}^2$$

$$V_{OV} = (v_{GS} - V_t) = 0.5 \text{ V}$$

$$g_{DS} = \frac{1}{1 \text{ kΩ}} = k'_n \frac{W}{L} V_{OV} \Rightarrow \frac{W}{L} = 5.15$$

$$L = 0.18 \text{ μm}, \text{ so } W = 0.93 \text{ μm}$$
A circuit designer intending to operate a MOSFET in saturation is considering the effect of changing the device dimensions and operating voltages on the drain current $I_D$. Specifically, by what factor does $I_D$ change in each of the following cases?

(a) The channel length is doubled.
(b) The channel width is doubled.
(c) The overdrive voltage is doubled.
(d) The drain-to-source voltage is doubled.

**Ex: 5.3**

$$I_D = \frac{1}{2} k \frac{W}{L} V^2_{ov}$$ in saturation

Change in $I_D$ is:

(a) double $L$, 0.5
(b) double $W$, 2
(c) double $V_{ov}$, $2^2 = 4$
(d) double $V_{DS}$, no change (ignoring length modulation)
An NMOS transistor is operating at the edge of saturation with an overdrive voltage $V_{OV}$ and a drain current $I_D$. If $V_{OV}$ is doubled, and we must maintain operation at the edge of saturation, what should $V_{DS}$ be changed to? What value of drain current results?

**Ans.** $2V_{OV}; 4I_D$

---

**Ex: 5.4** In saturation $V_{DS} \geq V_{OV}$, so $2V_{OV}$

\[
I_D = \frac{1}{2} k' \frac{W}{L} V_{OV}^2, \text{ so } 4I_D.
\]
For the circuit in Fig. E5.9, find the value of $R$ that results in $V_D = 0.8 \, \text{V}$. The MOSFET has $V_{tn} = 0.5 \, \text{V}$, $\mu_n C_{ox} = 0.4 \, \text{mA/V}^2$, $W/L = \frac{0.72 \, \mu\text{m}}{0.18 \, \mu\text{m}}$, and $\lambda = 0$.

Ans. $13.9 \, \text{k}\Omega$

Ex: 5.9

\[ +1.8 \, \text{V} \]
\[ R \]
\[ V_D \]

\[ Q_1 \]

\[ \frac{W}{L} = \frac{0.72 \, \mu\text{m}}{0.18 \, \mu\text{m}} = 4.0 \]

$\lambda = 0$

saturation mode ($v_{GD} = 0 < V_{tn}$)

\[ V_D = 0.8 \, \text{V} \Rightarrow 1.8 - I_D R_D \]

\[ I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_D - V_{tn})^2 = 72 \, \mu\text{A} \]

\[ \therefore R = \frac{1.8 - 0.8}{72 \, \mu\text{A}} = 13.9 \, \text{k}\Omega \]
Consider the amplifier circuit of Fig. 5.39(a) without the load resistance $R_L$ and with channel length modulation neglected. Let $V_{DD} = 5$ V, $V_i = 0.7$ V, and $k_n = 1$ mA/V². Find $V_{OV}$, $I_D$, $R_D$, and $R_G$ to obtain a voltage gain of 25 V/V and an input resistance of 0.5 MΩ. What is the maximum allowable input signal, $v_i$?

Ans. 0.319 V, 50.7 μA, 78.5 kΩ; 13 MΩ; 27 mV.

**Fig. 5.39(a)**

- $V_{DD} = +5$ V
- $R_D = 10kΩ$
- $R_L = 10kΩ$
- $R_G = 10^8Ω$
- $V_i = 0.7$ V
- $k_n = 1$ mA/V²

**Design for $A_v = \frac{v_o}{v_i}$**

$A_v = \frac{V_{DD} - V_i - I_D R_D}{V_i}$

$\therefore A_v = 25 = k_n V_{OV} R_D$

$R_{in} = \frac{v_i}{i_i} = \frac{v_i}{v_i - v_o}$

$\Rightarrow R_D = 26R_{in} = 13$ MΩ

$I_D R_D = \left( \frac{1}{2} k_n V_{OV}^2 \right) R_D$

$= \frac{1}{2} k_n R_D V_{OV} = 12.5 V_{OV}$

and

$V_{OV} = V_{DD} - V_i - I_D R_D = 4.3 - 12.5 V_{OV}$

$\therefore V_{OV} = 0.319$ V

$g_m = 319$ μA/V

$R_D = 78.5$ kΩ

$V_{DS} = V_{OV} + V_r$

$\tilde{v}_{DD} = 0 + 26\tilde{v}_i \approx V_r$

$\therefore |\tilde{v}_i| < \frac{V_r}{26} = 27$ mV.
Consider the circuit of Fig. 5.56 for the case $V_{DD} = V_{SS} = 10 \text{ V}$, $I = 0.5 \text{ mA}$, $R_G = 4.7 \text{ M}\Omega$, $R_D = 15 \text{ k}\Omega$, $V_i = 1.5 \text{ V}$, and $k'_n(W/L) = 1 \text{ mA/V}^2$. Find $V_{OV}$, $V_{GS}$, $V_G$, $V_S$, and $V_D$. Also, calculate the values of $g_m$ and $r_o$, assuming that $V_A = 75 \text{ V}$. What is the maximum possible signal swing at the drain for which the MOSFET remains in saturation?

**Ans.** See Fig. E5.37; without taking into account the signal swing at the gate, the drain can swing to $-1.5 \text{ V}$, a negative signal swing of $4 \text{ V}$.
Ex: 5.37

\( V_t = 1.5 \text{ V} \)

\( k_n \frac{W}{L} = 1 \text{ mA/V}^2 \)

\( V_A = 75 \text{ V}. \)

\( I_D = 0.5 \text{ mA} = \frac{1}{2} k_n \frac{W}{L} V_{OV}^2 \Rightarrow V_{OV} = 1.0 \text{ V}. \)

![Circuit Diagram]

\( V_{GS} = V_t + V_{OV} = 2.5 \text{ V} \)

\( V_G = 0 \)

\( V_S = -2.5 \text{ V}. \)

\( V_D = V_{DD} - I_D R_D = +2.5 \text{ V}. \)

\( g_m = k_n \frac{W}{L} V_{OV} = 1 \text{ mA/V} \)

\( r_O = \frac{V_A}{I_D} = 150 \text{ k\Omega} \)

\( V_{GD} - \hat{\theta}_{gd} = V_t \)

\(-\hat{\theta}_{gd} \equiv \hat{\theta_d} = V_t - V_{GD} = 4.0 \text{ V}. \)
For a depletion-type NMOS transistor with $V_t = -2$ V and $k_n' (W/L) = 2$ mA/V$^2$, find the minimum $V_{DS}$ required to operate in the saturation region when $V_{GS} = +1$ V. What is the corresponding value of $i_D$?

**Ans.** 3 V; 9 mA

**Ex: 5.43**

$V_{GS} = +1$ V, $V_+ = -2$ V

$V_{GS} - V_+ = 3$ V

TO OPERATE IN SATURATION REGION:

$V_{DS_{min}} = V_{GS} - V_+ = 3$ V

$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_+)^2$

$= \frac{1}{2} \times 2 \times 3^2 = 9$ mA
An NMOS transistor with $k_n = 1 \text{mA/V}^2$ and $V_t = 1 \text{V}$ is operated with $V_{GS} = 2.5 \text{V}$. At what value of $V_{DS}$ does the transistor enter the saturation region? What value of $I_D$ is obtained in saturation?

In saturation:

$$i_D = \frac{1}{2} K_u' \left( \frac{W}{L} \right) V_{OV}^2 = \frac{1}{2} K_u V_{OV}^2$$

$$i_D = \frac{1}{2} \times \frac{1 \text{mA}}{1 \text{V}^2} \times (1.5 \text{V})^2$$

$$i_D = (1.125 \text{ mA})$$
Problem

5.14 Consider an n-channel MOSFET with $t_{ox} = 9$ nm, $\mu_n = 500 \text{ cm}^2/\text{V} \cdot \text{s}$, $V_t = 0.7$ V, and $W/L = 10$. Find the drain current in the following cases:

(a) $v_{GS} = 5$ V and $v_{DS} = 1$ V
(b) $v_{GS} = 2$ V and $v_{DS} = 1.3$ V
(c) $v_{GS} = 5$ V and $v_{DS} = 0.2$ V
(d) $v_{GS} = v_{DS} = 5$ V

5.14 $t_{ox} = 9$ nm, $\mu_n = 500 \text{ cm}^2/\text{V}$,
$V_t = 0.7$ V, $\frac{W}{L} = 10$

$k_n = \mu_n C_{ox} = \mu_n \frac{\varepsilon_{ox}}{t_{ox}}$

$500 \times 10^{-4} \times \frac{3.45 \times 10^{-11}}{9 \times 10^{-9}} = 191.7 \frac{\mu A}{V^2}$

(a) triode region: $V_{DS} < V_{GS} - V_t$

$i_D = k_n \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$

$= 191.7 \times 10^{-6} \times 10$

$\left[ (5 - 0.7) \times 1 - \frac{1}{2} \times 1^2 \right] = 7.3 \text{ mA}$

(b) saturation region: $V_{DS} > V_{GS} - V_t$

$i_D = \frac{1}{2} \times 191.7 \times 10^{-6} \times 10 \times (2 - 0.7)^2$

$= 1.62 \text{ mA}$

(c) triode region: $V_{DS} < V_{GS} - V_t$

$i_D = 191.7 \times 10^{-6} \times 10 \left[ (5 - 0.7) \times 0.2 - \frac{1}{2} (0.2)^2 \right]$

$= 1.61 \text{ mA}$

(d) saturation region: $V_{DS} > V_{GS} - V_t$

$i_D = \frac{1}{2} \times 191.7 \times 10^{-6} \times 10 \times (5 - 0.7)^2$

$= 17.7 \text{ mA}$
An NMOS transistor having $V_t = 1$ V is operated in the triode region with $v_{DS}$ small. With $V_{GS} = 1.5$ V, it is found to have a resistance $r_{DS}$ of 1 kΩ. What value of $V_{GS}$ is required to obtain $r_{DS} = 200$ Ω? Find the corresponding resistance values obtained with a device having twice the value of $W$.

5.17 Eq.4.13: $r_{DS} = \left[ k \frac{W}{nL} (V_{GS}-V_t) \right]^{-1}$

Therefore:

$$\frac{r_{DS1}}{r_{DS2}} = \frac{V_{GS2}-V_t}{V_{GS1}-V_t} \Rightarrow \frac{1000}{200} = \frac{V_{GS2}-1}{1.5-1}$$

$\Rightarrow V_{GS2} = 3.5$ V

Now for a device with twice the width:

$$\frac{r_{DS1}}{r_{DS2}} = \frac{W_2(V_{GS2}-V_t)}{W_1(V_{GS2}-V_t)}$$

for $V_{GS} = 1.5$ V

$$\frac{r_{DS1}}{r_{DS2}} = 2 \Rightarrow r_{DS2} = \frac{1000}{2} = 500 \, \Omega$$

for $V_{GS} = 3.5$ V $r_{DS2} = \frac{200}{2} = 100 \, \Omega$
Problem

5.18 A particular enhancement MOSFET for which $V_t = 0.5$ V and $k'_n(W/L) = 0.1 \text{mA/V}^2$ is to be operated in the saturation region. If $i_D$ is to be 12.5 $\mu$A, find the required $v_{GS}$ and the minimum required $v_{DS}$. Repeat for $i_D = 50 \mu$A.

5.18 $V_{th} = 0.5$ V

$k'_n \frac{W}{L} = 0.1 \text{mA/V}^2$

Saturation mode

$v_{DS} \geq (v_{GS} - V_{th})$

for $i_D = 12.5 \mu$A

$v_{GS} = 1.0 \text{ V and } v_{DS} \geq 0.5 \text{ V}$

for $i_D = 50 \mu$A

$v_{GS} = 1.5 \text{ V, and } v_{DS} \geq 1.0 \text{ V}$
Problem

5.22 For an NMOS transistor, for which $V_t = 0.5$ V, operating with $v_{GS}$ in the range of 0.8 V to 1.8 V, what is the largest value of $v_{DS}$ for which the channel remains continuous?

$5.22 \ V_t = 0.5 \ V.$

$0.8 \leq v_{GS} \leq 1.8 \ V.$

largest $v_{DS}$ for ohmic operation?

$v_{DS} \leq v_{OV} = v_{GS} - V_t = 0.3 \sim 1.3 \ V.$

$\therefore v_{DS} \leq 0.3 \ V$ will ensure ohmic mode
5.47 The transistor in the circuit of Fig. P5.47 has \( k_n' = 0.4 \text{ mA/V}^2 \), \( V_t = 0.5 \text{ V} \), and \( \lambda = 0 \). Show that operation at the edge of saturation is obtained when the following condition is satisfied:

\[
\left( \frac{W}{L} \right) R_D = 1.5 \text{ k} \Omega
\]

![Figure P5.47](image)

\[
k_n = 0.4 \text{ mA/V}^2
\]

\[
V_t = 0.5 \text{ V},
\]

\[
\lambda = 0
\]

sat. boundary \( V_{GD} = 0.5 \text{ V} \), \( = I_D R_D \)

\[
0.5 \text{ V} = \frac{1}{2} k_n' \frac{W}{L} (1.8 - 0.5)^2 R_D
\]

\[
\therefore \frac{W}{L} R_D = 1.48 \text{ k} \Omega
\]
Both MOS

\[ V_T = 0.5 \text{ V} \]

\[ U_m(\Delta V) = 250 \mu A / \text{V}^2 \]

\[ \Delta = 0 \]

\[ L_1 = L_2 = 0.25 \text{ mm} \]

What is value of gate width of both MOS and value of \( R \) to obtain values of voltages and current indicated?

**Figure P5.50**

\begin{align*}
L_1 = L_2 &= 0.25 \text{ mcm} \\
R &= \frac{2.5 - 1.8}{0.25 \text{mA}} = 2.8 \text{ k}\Omega

d \text{ for } Q_1, \\
0.25 \text{mA} &= \frac{1}{2} (250 \mu A / \text{V}^2) \frac{W}{L_1} (1 - 0.5)^2 \\
\therefore W_1 &= 8L_1 = 2 \text{ mcm} \\
d \text{ for } Q_2, \\
0.25 \text{mA} &= \frac{1}{2} (250 \mu A / \text{V}^2) \\
\frac{W}{L_2} (1.8 - 1.0 - 0.5)^2 \\
\therefore W_2 &= 22.2L_2 = 5.6 \text{ mcm}
\end{align*}
5.57 For each of the circuits shown in Fig. P5.57, find the labeled node voltages. The NMOS transistors have $V_t = 1$ V and $k'_n W/L = 5$ mA/V$^2$. 

![Diagrams of circuits](image)

**Figure P5.57**
5.57 (a) \( V_t = 1 \text{V}, \quad k_n \frac{W}{L} = \frac{5 \text{mA}}{V^2} \lambda = 0 \)

\( Q_1 \) is in saturation
\( Q_2 \) assume sat.
\( V_2 = -V_{GS} = -2.5 + I_D 1\text{k} \)

\(-V_{GS} = -2.5 + (1) \left( \frac{1}{2} \right) (5) [V_{GS} - 1]^2 \)

\( 0 = 2.5V_{GS}^2 - 4V_{GS} + 0 \)
\( V_{GS} = +1.6 \text{V} \) (0, bad root < \( V_t \))
\( I_D = 0.90 \text{ mA} \)
\( V_{GS1} = +1.6 \text{V} \)
\( V_1 = +2.5 - V_{GS1} = +0.9 \text{ V} \)
\( V_{GD2} = -0.9 < V_t \quad \therefore \) \( Q_2 \) sat.
\( V_2 = -1.6 \text{V} \).

Both \( Q_1 \) and \( Q_2 \) in sat.

\( V_{GD1} = V_{GD2} = 0 \)
\( V_{GS} = +1.6 \text{V} \) (bad root < \( V_t \))
\( I_D = 0.90 \text{mA} = \frac{1}{2} \left( \frac{5 \text{mA}}{V^2} \right) [1.6 - 1]^2 \)
\( V_1 = +5 - (1k)I_D = +4.1 \text{V} \).
\( V_2 = V_1 - V_{GS} = +2.5 \text{V} \).
\( V_3 = V_2 - V_{GS} = (1k)I_D = 0.9 \text{V} \).
For the NMOS amplifier in Fig. P5.76, replace the transistor with its T equivalent circuit, assuming $\lambda = 0$. Derive expressions for the voltage gains $v_d/v_i$ and $v_{ad}/v_i$.

\[ v_i = (g_m v_{gs}) \left( \frac{1}{g_m} + R_S \right) \]

\[ v_d = -g_m v_{gs} R_D \]

\[ v_S = +g_m v_{gs} R_S \]

\[ \frac{v_S}{v_i} = \frac{R_S}{1 + R_S} = \frac{+g_m R_S}{1 + g_m R_S} \]

\[ \frac{v_d}{v_i} = \frac{-R_D}{1 + R_S} = \frac{-g_m R_D}{1 + g_m R_S} \]
Figure P5.79 shows a discrete-circuit amplifier. The input signal $v_{\text{sig}}$ is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite).

(a) If the transistor has $V_t = 1\,\text{V}$, and $k_n = 2\,\text{mA}/\text{V}^2$, verify that the bias circuit establishes $V_{GS} = 2\,\text{V}$, $I_D = 1\,\text{mA}$, and $V_D = +7.5\,\text{V}$. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.

(b) Find $g_m$ and $r_o$ if $V_A = 100\,\text{V}$.

(c) Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.

(d) Find $R_{in}$, $\frac{v_{gs}}{v_{\text{sig}}}$, $\frac{v_o}{v_{gs}}$, and $\frac{v_o}{v_{\text{sig}}}$.

---

5.79 $V_t = 1\,\text{V}$, $k_n = \frac{W}{L} = 2\,\text{mA}/\text{V}^2$

(a) dc analysis $V_G = \frac{5}{15} \cdot 15 = 5\,\text{V}$, assume

$I_D = 1\,\text{mA}$

$V_S = 3\,\text{V}$, $V_{GS} = 2\,\text{V}$, $V_{0V} = 1\,\text{V}$.

$I_D = \frac{1}{2}k'_nV_{0V}^2 = 1\,\text{mA}$ (check)
\[ V_D = V_{DD} - I_D R_D = 7.5 \text{V}. \]

(b) \( r_0 = \frac{V_A}{I_D} = \frac{100 \text{ V}}{1 \text{ mA}} = 100 \text{ k}\Omega \)

\[ g_m = \sqrt{2 k_n I_D} = 2 \text{ mS} \]

(c) 

\[ R_{SIG} = 100K \]

\[ v_{SIG} \]

\[ R_G = 3.33 \text{m}\Omega \]

\[ v_{gs} \]

\[ g_m v_{gs} \]

\[ D \]

\[ v_0 \]

\[ S \]

(d) \( R_{in} = R_G = 3.33 \text{M}\Omega \)

\[ \frac{v_{gs}}{v_{sig}} = \frac{R_{in}}{R_{sig} + R_{in}} = 0.97 \]

\[ \frac{v_0}{v_{gs}} = -g_m (r_0 || R_D || R_L) = -8.2 \]

\[ \frac{v_0}{v_{sig}} = -8.0 \]
5.93 A CG amplifier using an NMOS transistor for which \( g_m = 4 \text{ mA/V} \) has a 5-k\( \Omega \) drain resistance \( R_D \) and a 5-k\( \Omega \) load resistance \( R_L \). The amplifier is driven by a voltage source having a 500 \( \Omega \) resistance. What is the input resistance of the amplifier? What is the overall voltage gain \( G_V \)? By what factor must the bias current \( I_D \) of the MOSFET be changed so that \( R_{in} \) matches \( R_{sig} \)?

\[
5.93 \quad R_{in} = \frac{1}{g_m} = 250 \Omega
\]

\[
G_V = \frac{v_D}{v_{sig}} = \frac{R_{in}}{R_{sig} + R_{in}} g_m (R_D || R_L) = +3.3
\]

\[
\frac{1}{g_m} = \frac{1}{2 k_n I_D}, \text{ so for } \frac{1}{g_m} = R_{sig}, \quad g_m \text{ must decrease to } \frac{1}{2}, \text{ and } I_D \text{ must decrease to } \frac{1}{4}
\]
The NMOS transistor in the CS amplifier shown in Fig. P5.112 has $V_T = 0.7$ V and $V_A = 50$ V.

(a) Neglecting the Early effect, verify that the MOSFET is operating in saturation with $I_D = 0.5$ mA and $V_{OV} = 0.3$ V. What must the MOSFET's $k_n$ be? What is the dc voltage at the drain?

(b) Find $R_{in}$ and $G_V$.

(c) If $v_{sig}$ is a sinusoid with a peak amplitude $\hat{v}_{sig}$, find the maximum allowable value of $\hat{v}_{sig}$ for which the transistor remains in saturation. What is the corresponding amplitude of the output voltage?

(d) What is the value of resistance $R_s$ that needs to be inserted in series with capacitor $C_S$ in order to allow us to double the input signal $\hat{v}_{sig}$? What output voltage now results?

5.112

$V_T = 0.7$ V.

$V_A = 50$ V.
a) with $I_D = 0.5$ mA

$V_G = +2$ V $V_S = 1$ V. $V_{GS} = +1$ V.

$V_{OV} = 0.3$ V

$0.5$ mA $= \frac{1}{2} k_n V_{ov}^2 \Rightarrow k_n = \frac{11.1 \text{mA}}{V^2}$

$V_D = 5 - (5 \text{ K})(0.5 \text{ mA}) = +2.5$ V.

$V_{GD} = -0.5V < V_T$ : Satsuration

b) $R_{in} = 200 \text{ K} \parallel 300 \text{ K} = 120 \text{ k}\Omega$

$G_V = \frac{\nu_o}{\nu_{sig}} = -\frac{R_{in}}{120 \text{ K} - R_{in}} g_m$

$(5 \text{ K} \parallel r_o \parallel 5 \text{ K})$

$g_m = \frac{2I_D}{V_{ov}} = 3.33\text{mS}$

$r_o = \frac{V_A}{I_D} = 100 \text{ k}\Omega$

$G_V = -4.1$

c) $\nu_{sig} = \hat{\nu}_{sig} \sin \omega t$

$g_m(5\text{ K} \parallel 5\text{ K} \parallel 100\text{ K}) = 8.12$

$$V_{gd} + V_{GD} = \hat{\nu}_0 + \frac{\hat{\nu}_0}{8.12} - 0.5 \leq V_T = 0.7 \text{V}. \quad \hat{\nu}_{o, \text{max}} = 1.07 \text{ V}_{pk}$$

$\hat{\nu}_{o, \text{max}} = \frac{\hat{\nu}_o \max}{8.12} = 132 \text{ mV}_{pk}$

$\hat{\nu}_{o, \text{max}} = \frac{\hat{\nu}_o \max}{4.1} = 261 \text{ mV}_{pk}$

d) Add $R_s = \frac{1}{g_m} = 300 \ \Omega$,

then $\nu_{gs} = \frac{\nu_o}{1 + g_m R_s} = \frac{\nu_o}{2}$

$$\frac{g_m R_s}{1 + g_m R_s} = \left| \frac{\nu_o}{\nu_o} \right| = 4.06$$

$\hat{\nu}_o + \frac{\hat{\nu}_o}{4.06} - 0.5 \leq 0.7 \text{ V}.$

$\Rightarrow \hat{\nu}_{o, \text{max}} = 0.96 \text{ V}.$