DQE--Fall 2007—Computer Architecture

1. (50 points)

Consider a generic byte addressable memory hierarchy consisting of the following: a 4MB virtual address space, a direct-mapped L1 I-cache containing 256 blocks with each block containing 64 addresses, a 3-way set-associate L1 D-cache containing 384 blocks with each block containing 64 addresses, a fully associative L2 cache containing 1M addresses with 128 bytes in each block, segmented-paged virtual memory (512MB physical memory space, 16 segments, 8K pages, LRU replacement, and a 2GB swap disk). Assume that the L1 I-cache has a hit time of 1 cycle, that the L1 D-cache has a 2 clock cycle hit time, that the L2 cache has a 20 cycle hit time, and that main memory has a 200 cycle hit time. Assume that the L1 D-cache uses a write back cache update policy and that the L2 caches employ a write through cache update policy. Show the effect that adding a victim buffer has on the average memory access time of the system.

2. (50points)

Assume a deeply pipelined processor that implements a branch target buffer for conditional branches (only); that the (i) misprediction penalty is 5 cycles, (ii) buffer miss penalty is 7 cycles, (iii) branch frequency is 23%, (iv) prediction accuracy is 84%, and (v) prediction hit rate is 93%. Develop a formula that characterizes the performance of this machine against a machine with a fixed 3-cycle branch penalty.