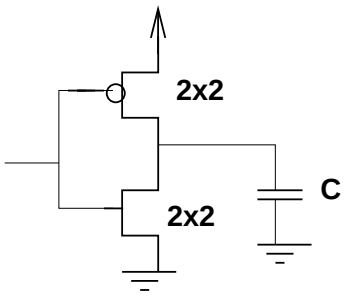
1. (50 points)

   The CMOS inverter shown in the following figure has a rise time of 4 ns and fall time of 2 ns. Using the same technology, design a *minority-of-three* circuit driving the same load C such that its worst case rise and fall times are within 2 ns. The *minority-of-three* circuit has three inputs and one output such that the output is low (high) whenever at least two of the inputs assume high (low). Clearly show the dimensions of all the transistors in your circuit.



2. (50 points)

A precharge bus in a CMOS circuit has an effective capacitance of 10pF. At some point in a clock cycle, N flip-flops need to simultaneously sample the charge on the bus. Each flip-flop is connected to the bus through a transmission gate which is used to enable the sampling. The input load of each flip-flop is 0.1pF (ignoring the transmission gate). Assuming that the bus is precharged to 5 volts, calculate, in terms of N, the final voltage of the bus after the sampling. Is this design acceptable for any N?. If not, what's a reasonable upper bound on N for the design to be acceptable? For larger values of N, suggest a more reliable way of connecting the N flip-flops to the same bus. Using your suggested method, determine the final voltage of the bus after sampling assuming that it was precharged to 5 volts.