Boundary Scan

- Objectives
- History
- Family of 1149
- Architecture
- Bus Protocol
- Boundary scan cell
- TAP controller
- Instruction set
- Boundary Scan Description Language

Objectives

- Standards for board level testing; can be used to test

  1. chips
  2. chip interconnections
  3. modules
  4. module interconnections
  5. subsystems
  6. systems
  7. Multi-Chip Modules

History

- 1985: Joint European Test Action Group (JETAG, Philips)
- 1986
  - VHSIC Element-Test & Maintenance (ETM) bus standard (IBM *et al.*)
  - VHSIC Test & Maintenance (TM) Bus structure (IBM *et al.*)
- 1988: Joint Test Action Group (JTAG) proposed Boundary Scan Standard
- 1990
  - Boundary Scan approved as IEEE Std. 1149.1-1990
  - Boundary Scan Description Language (BSDL) proposed by HP
- 1993: 1149.1a-1993 approved to replace 1149.1-1990
- 1994: 1149.1b BSDL approved
- 1995: 1149.5 approved
- 1999: 1149.4 approved

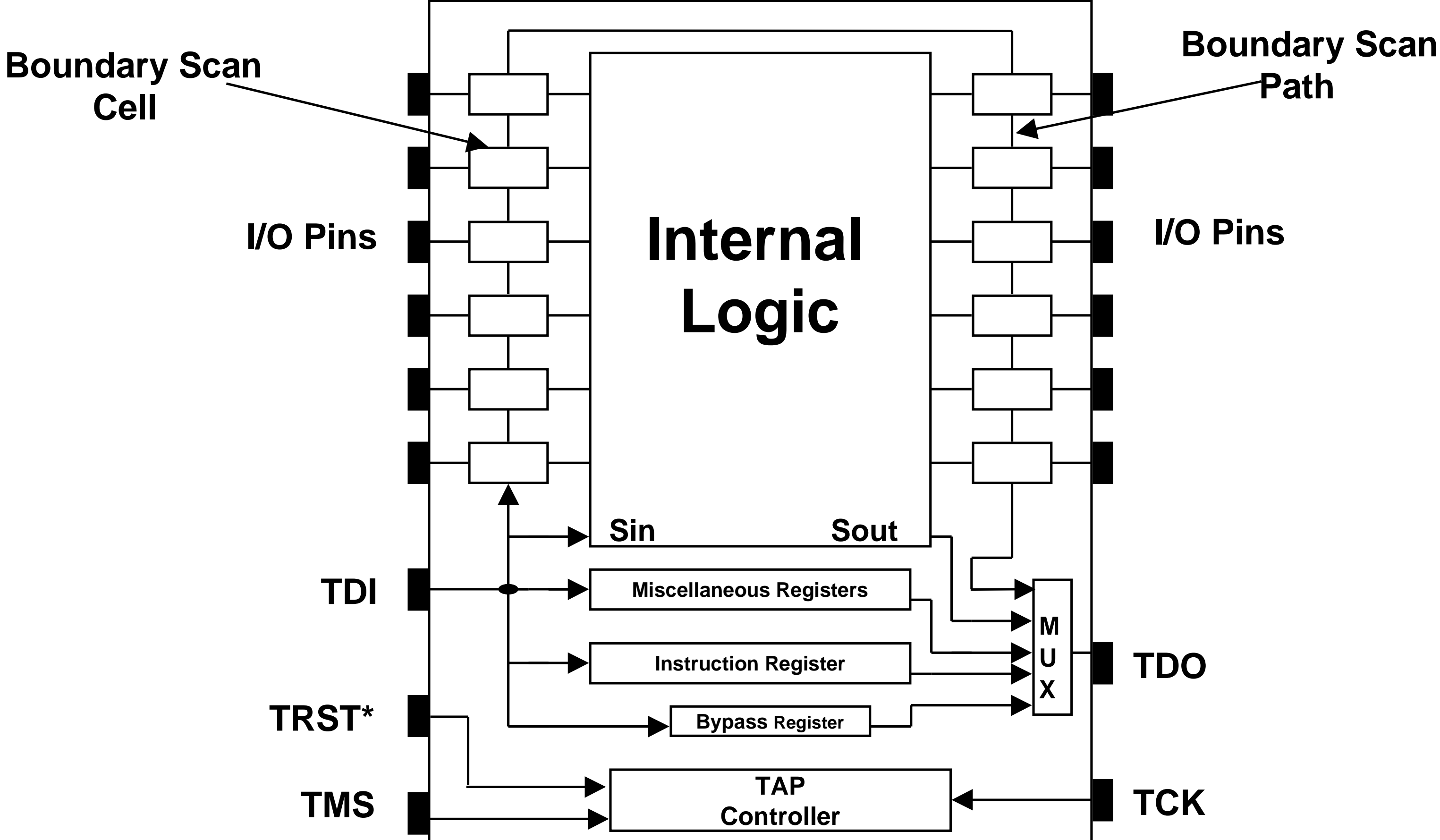
Overview of P1149 Family

Number	Title	Status
1149.1	Testing of digital chips and interconnections between chips	Std. 1149.1-1990 Std. 1149.1a-1993 Std. 1149.1b-1994 (BSDL)
1149.2	Extended Digital Serial Interface	Near completion
1149.3	Direct Access Testability interface	Discontinue
1149.4	Mixed-Signal Test Bus	Std. 1149.4-1999
1149.5	Standard Module Test and Maintenance (MTM) Bus Protocal	Std. 1149.5-1995
1149	Unification	Not yet started

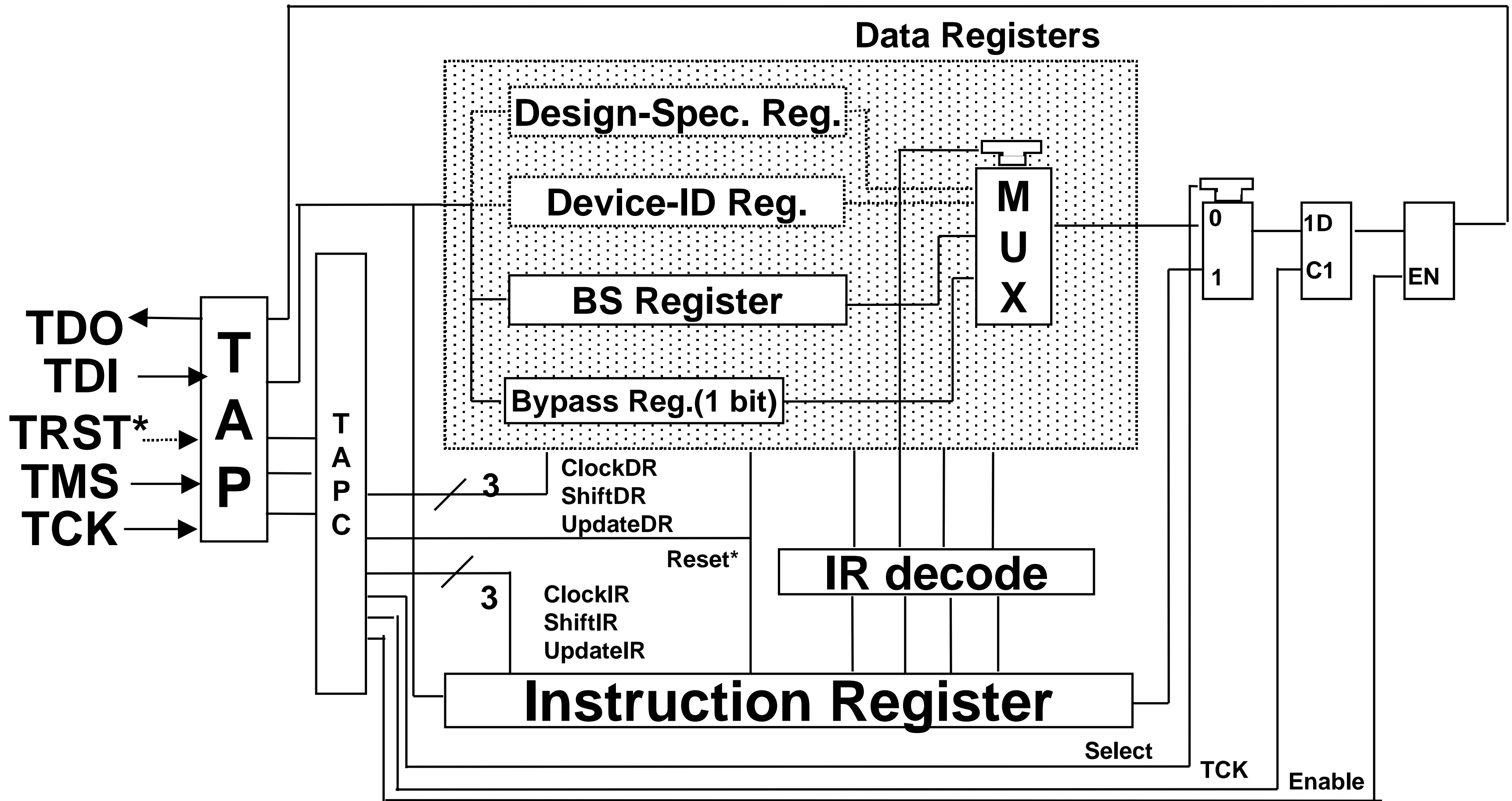
1149.1-1990, 1149.1a-1993

- Testing of chips and interconnections on board
- For digital circuits
- Most successful among 1149 family
- Widely used in industry, e.g., in advanced CPU, HDTV, satellite system, etc.

Basic Chip Architecture for 1149.1



Boundary Scan Circuitry in a Chip



Hardware Components of 1149.1

- **TAP (Test Access Port) :**

  TMS, TCK, TDI, TDO, TRST* (optional)

- **TAP Controller :**

  A finite state machine with 16 states
  Input : TCK, TMS
  Output : 9 or 10 signals included ClockDR, UpdateDR, ShiftDR, ClockIR, UpdateIR, ShiftIR, Select, Enable, TCK and the optional TRST*.

- **IR (Instruction Register)**

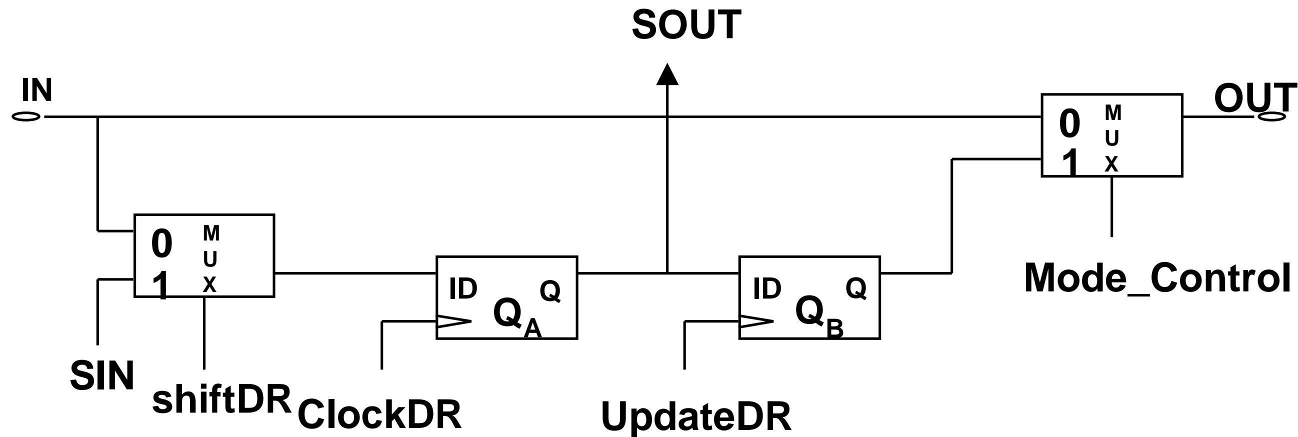
- **TDR (Test Data Registers) :**

  Mandatory: Boundary scan register and Bypass register
  Optional: Device-ID register, Design-Specific registers, etc.

Bus Protocol

- Signals
  - TDI: Test Data In
  - TDO: Test Data Out
  - TMS: Test Mode Selection
  - TCK: Test Clock
  - TRST* (optional): Test Reset
- Basic operations
  - Instruction sent (serially) over TDI into instruction register.
  - Selected test circuitry configured to respond to instruction.
  - Test instruction executed.
  - Test results shifted out through TDO; new test data on TDI may be shifted in at the same time.

A Typical Boundary Scan Cell



Operation modes:

1. Normal: Mode_Control=0;

   IN->OUT

2. Scan: ShiftDR=1,ClockDR;

   TDI->...->SIN->SOUT->...TDO

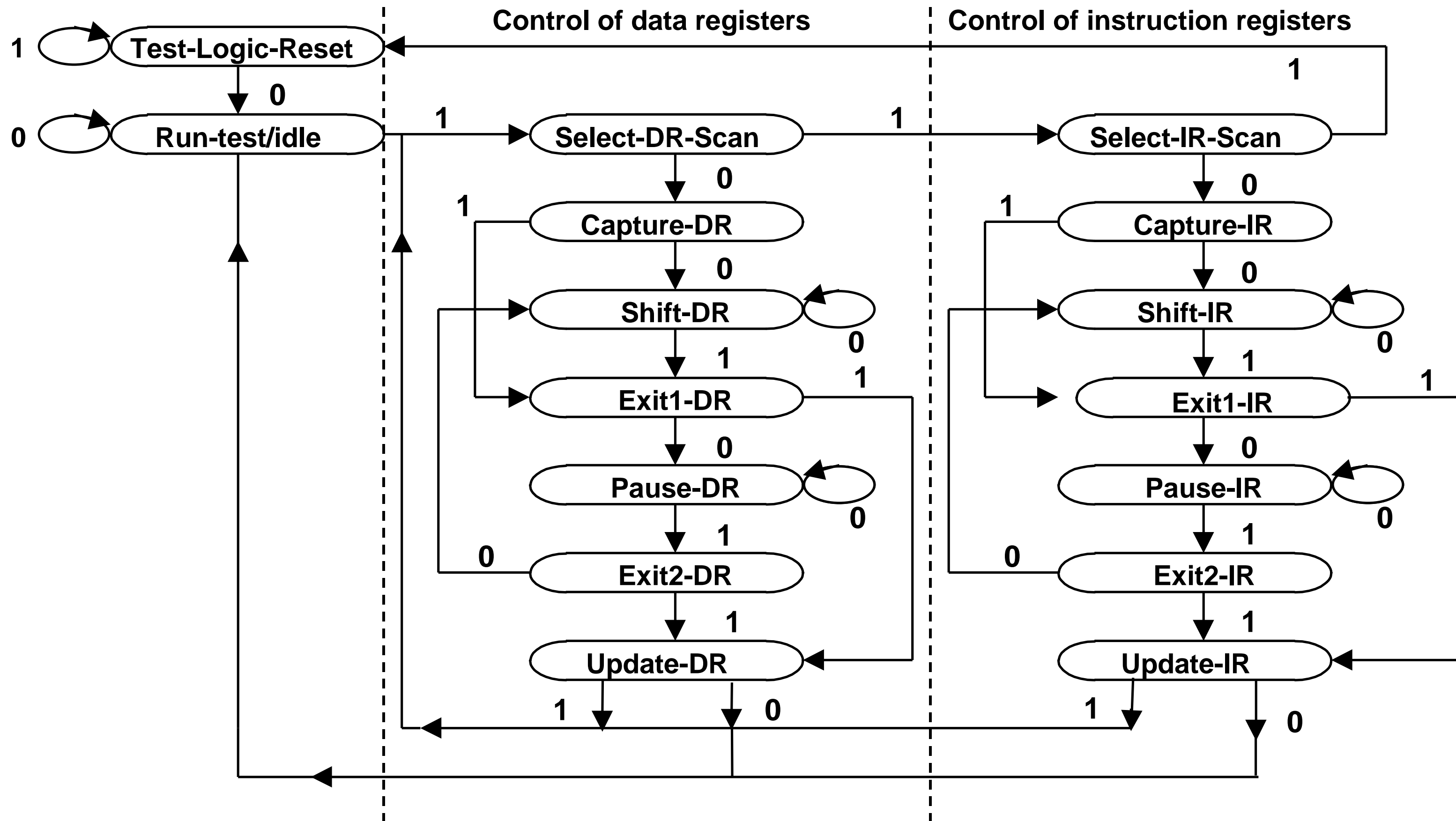
3. Capture: ShiftDR=0, ClcokDR;

   IN-> Q_A, OUT driven by IN or Q_B

4. Update: Mode_Control=1, UpdateDR;

   Q_A->OUT

State Diagram of TAP Controller



States of TAP Controller

- Test-Logic-Reset: normal mode
- Run-Test/Idle: wait for internal test such as BIST
- Select-DR-Scan: initiate a data-scan sequence
- Capture-DR: load test data in parallel
- Shift-DR: load test data in series
- Exit1-DR: finish phase-1 shifting of data
- Pause-DR: temporarily hold the scan operation (allow the bus master to reload data)
- Exit2-DR: finish phase-2 shifting of data
- Update-DR: parallel load from associated shift registers

Timing of instruction scan

TCK

TMS 0 1 1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 1 0 0 0 0

Control State: Test-Logic-Reset | Run-test/Idle | Select-DR-Scan | Select-IR-Scan | Capture-IR | Shift-IR | Exit1-IR | Pause-IR | Exit2-IR | Shift-IR | Exit1-IR | Update-IR | Run-Test/Idle

TDI

Data input to IR

IR shift-register

Parallel output of IR: IDCODE | New instruction

Data input to TDR

TDR shift-register

Parallel output of TDR: Old data

Register selected: Instruction register

TDO enable: Inactive | Active | Inactive | Active | Inactive

TDO

= Don't care or undefined

Timing of data scan

TCK

TMS 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1 1 0 0 0 1 1

Control State: Run-Test/Idle, SelectDR-Scan, Capture-DR, Shift-DR, Exit1-DR, Pause-DR, Exit2-DR, Shift-DR, Exit1-DR, Update-DR, Run-Test/Idle, SelectDR-Scan, SelectIR-Scan, Test-Logic-Reset

TDI

Data input to IR

IR shift-register

Parallel output of IR: Instruction, IDCODE

Data input to TDR

TDR shift-register

Parallel output of TDR: Old data, New data

Instruction Register: Test data register

TDO enable: Inactive, Active, Inactive, Active, Inactive

TDO

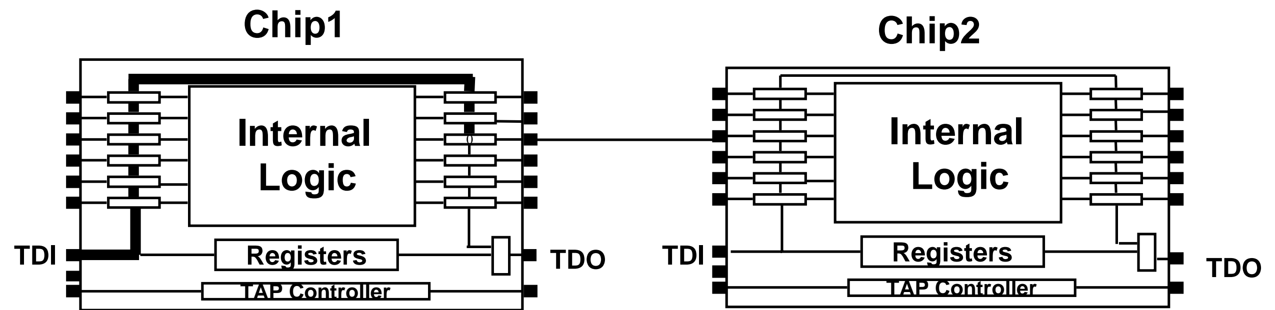
= Don't care or undefined

Instruction Set

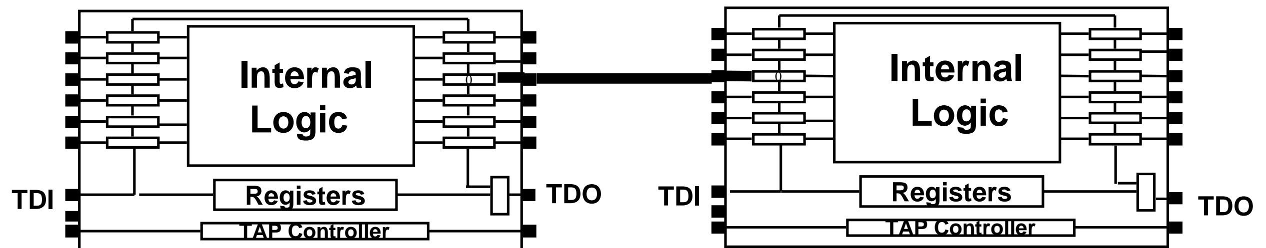
- **EXTEST:**
  - Test interconnection between chips of board
- **SAMPLE/PRELOAD:**
  - Sample and shift out data or shift in data only
- **BYPASS:**
  - Bypass data through a chip
- **Optional :**
  - INTEST, RUNBIST, CLAMP, IDCODE, USERCODE, HIGH-Z, etc.

EXTEST

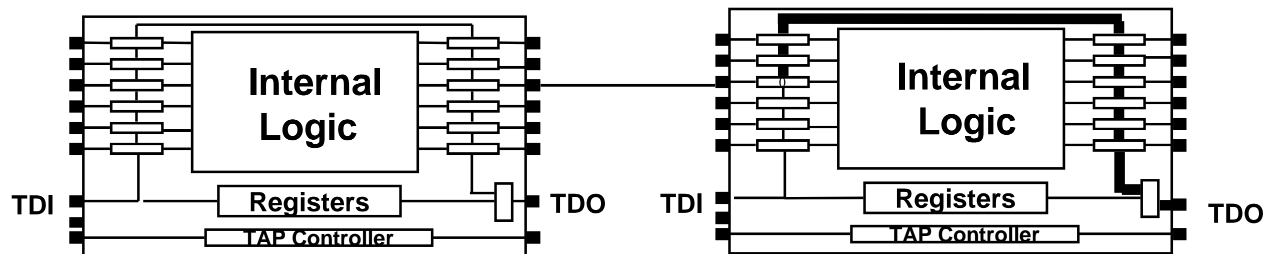
1. Shift-DR (Chip1)



2. Update-DR (Chip1)
3. Capture-DR (Chip2)

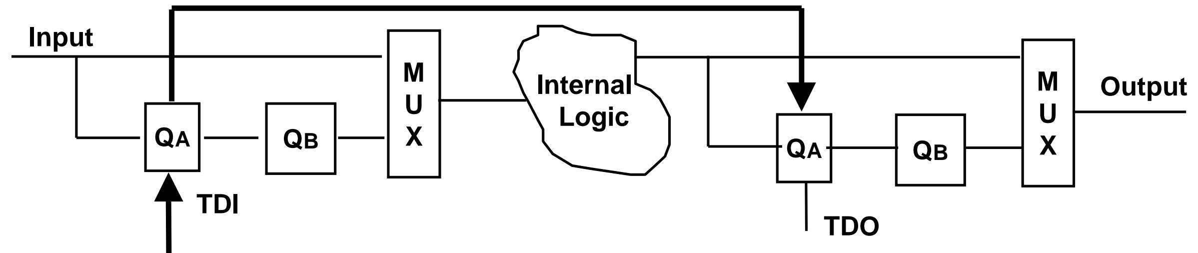


4. Shift-DR (Chip2)

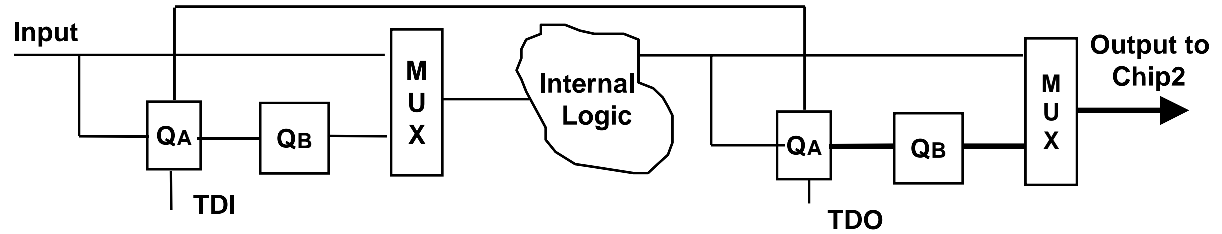


EXTEST

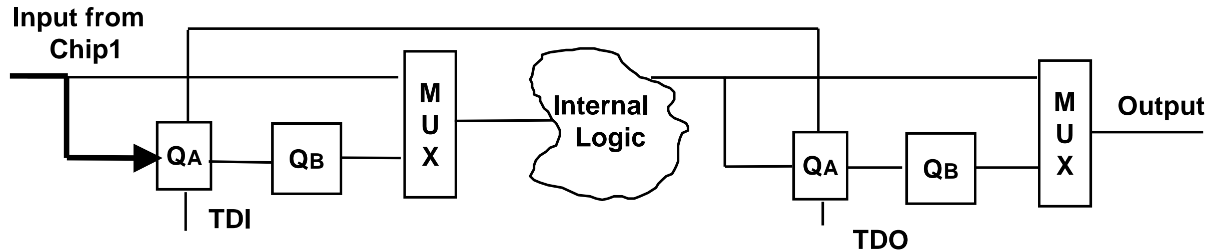
1. Shift-DR (Chip1)



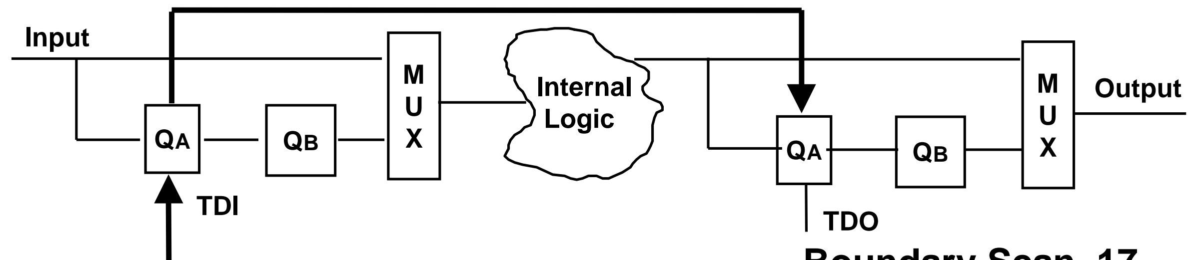
2. Update-DR (Chip1)



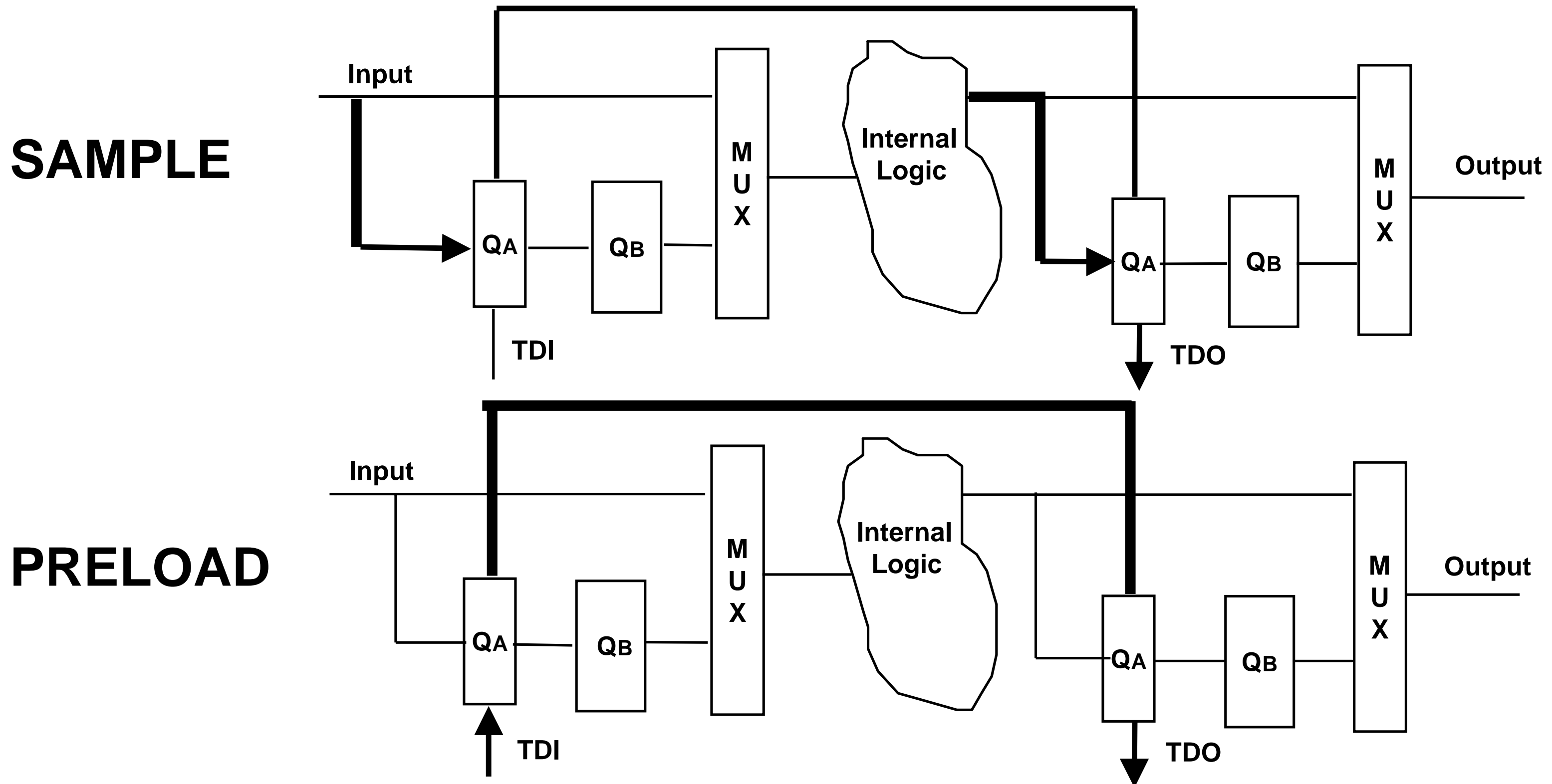
3. Capture-DR (Chip2)



4. Shift-DR (Chip2)



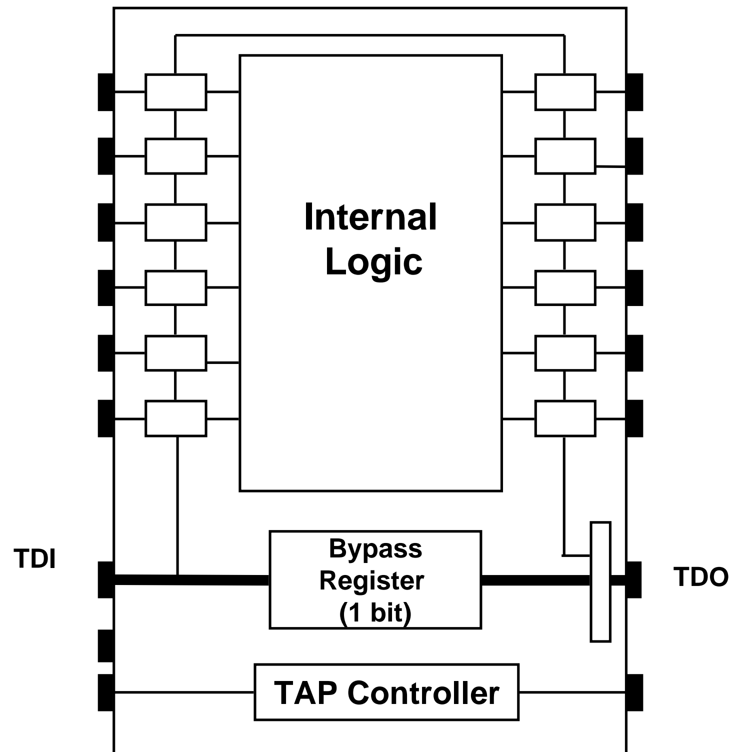
SAMPLE/PRELOAD



Sample/Preload is one instruction that allows

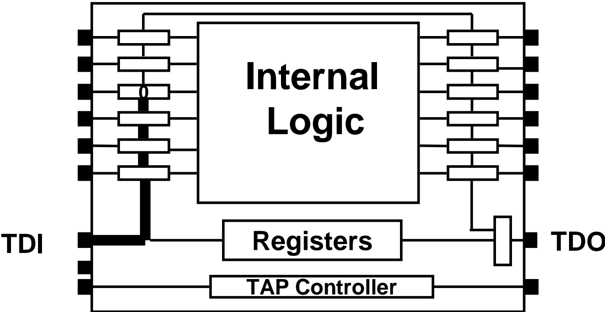
1. Sample and shift (out) or
2. Shift (in) only

BYPASS

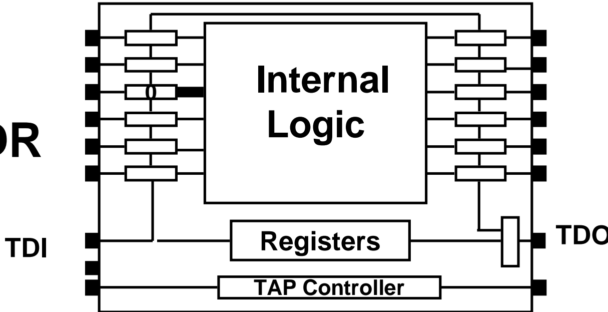


INTEST

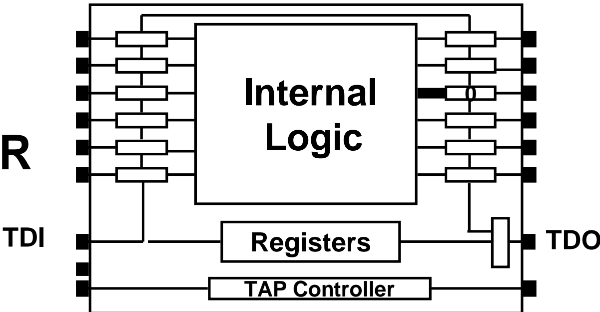
1.Shift-DR



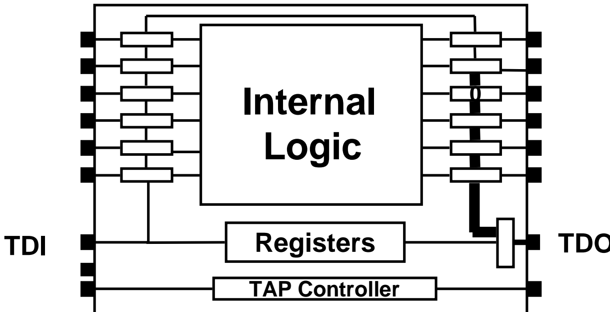
2.Update-DR



3.Capture-DR



4. Shift-DR



INTEST

1. Shift-DR

Input, QA, QB, MUX, Internal Logic, QA, QB, MUX, Output, TDI, TDO

2. Update-DR

Input, QA, QB, MUX, Internal Logic, QA, QB, MUX, Output, TDI, TDO

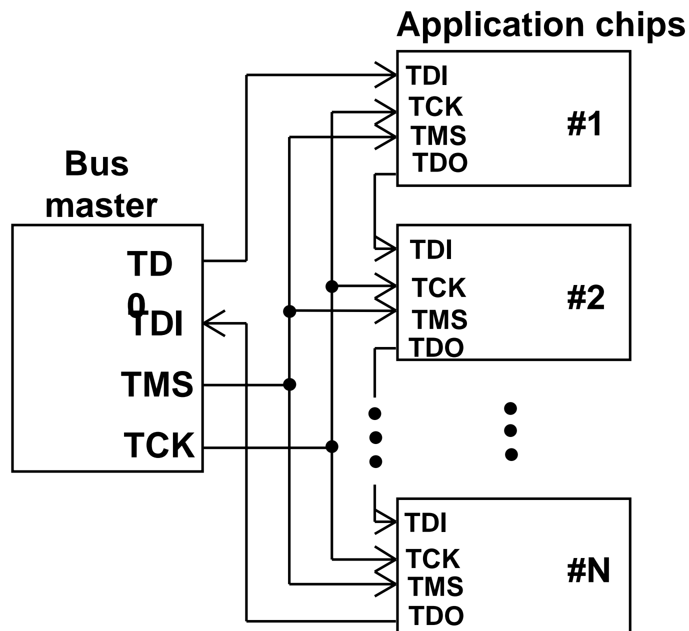
3. Capture-DR

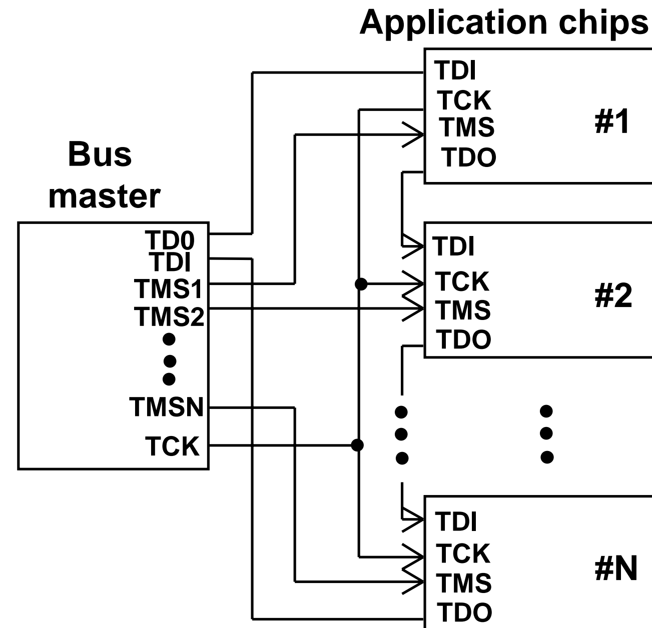
Input, QA, QB, MUX, Internal Logic, QA, QB, MUX, Output, TDI, TDO

4. Shift-DR

Input, QA, QB, MUX, Internal Logic, QA, QB, MUX, Output, TDI, TDO

Test Bus Configuration



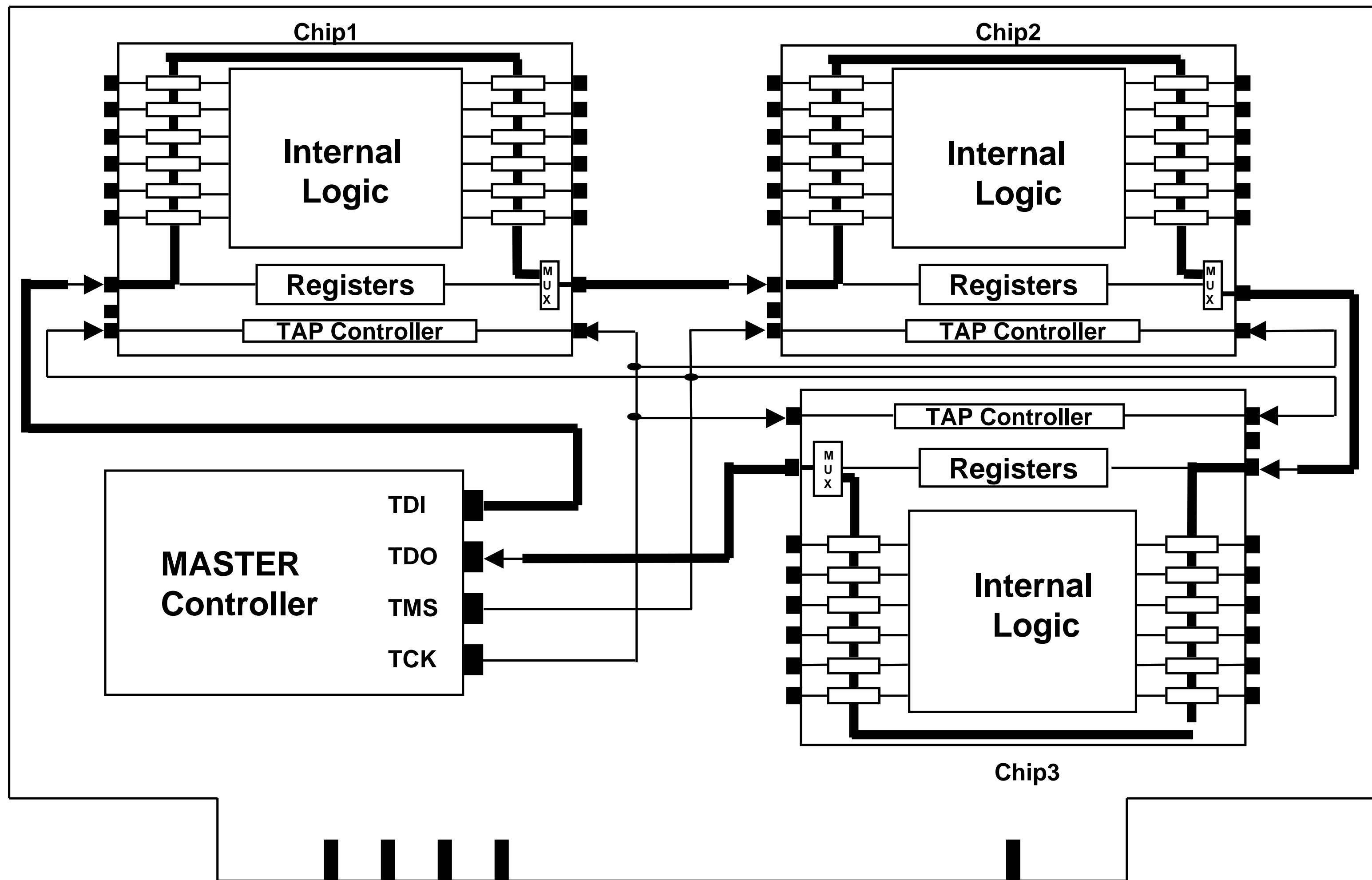


Ring configuration

Star configuration

A Printed Circuit Board with 1149.1

(Ring configuration, test controller on board)



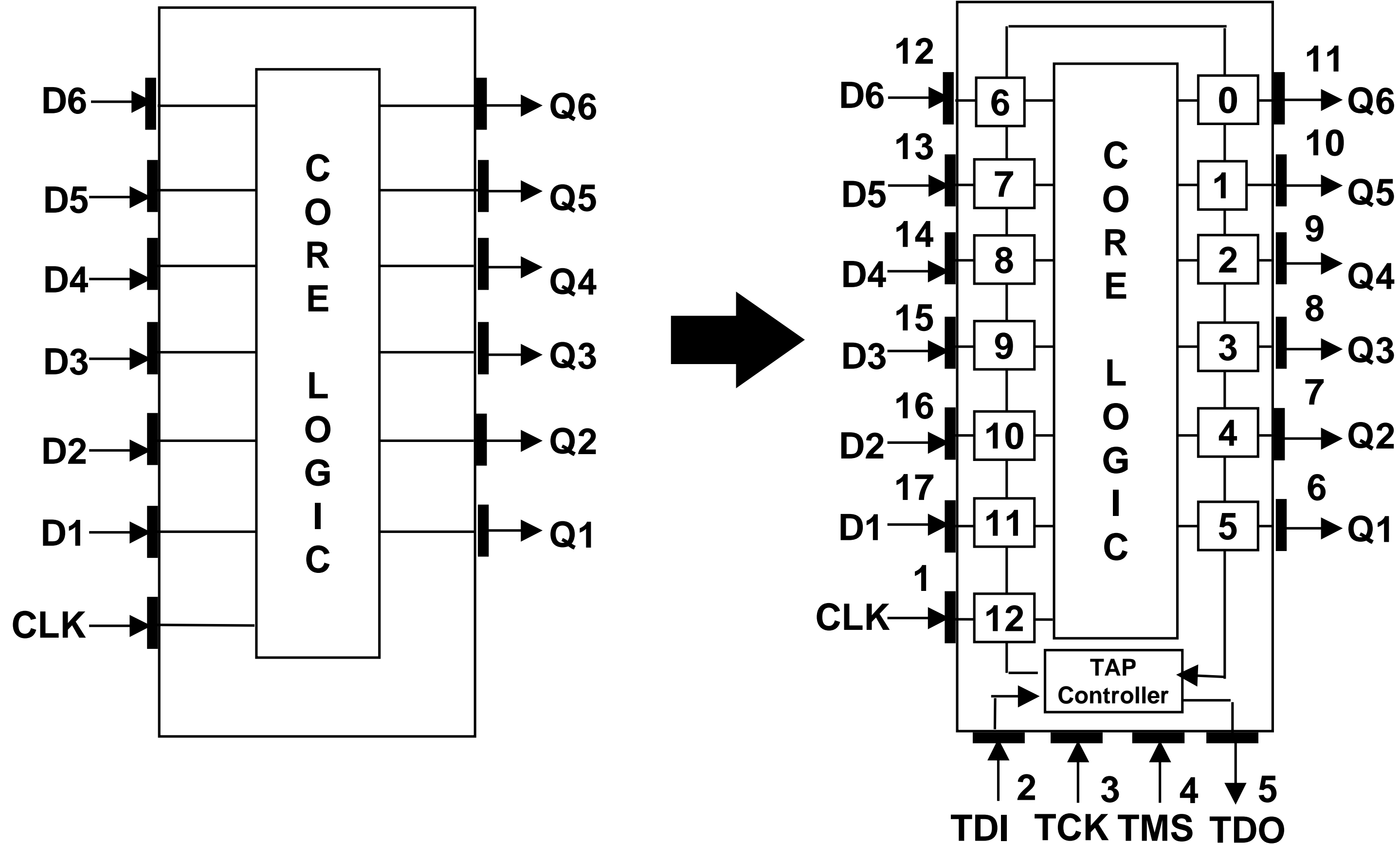
Boundary Scan Description Language (BSDL)

- Now the IEEE 1149.1b standard
- Purposes:
  - To provide a standard description language for boundary scan devices.
  - To simplify the design work for boundary scan---automated synthesis is possible.
  - To promote consistency throughout ASIC designers, device manufacturers, foundries, test developers and ATE manufacturers.
  - For easy incorporation into software tools for test generation, analysis and failure diagnosis.
  - To reduce possibility of human error when employing boundary scan in a design.

Features of BSDL

- BSDL describes the testability features of boundary scan devices which are compatible with 1149.1.
- It's a subset of VHDL.
- Elements of a design which are absolutely mandatory for the 1149.1 and system-logic are not included in the language.
  - Examples: BYPASS register, TAP controller, etc.
- BSDL may be used in a full or in a partial VHDL environment.

A Complete Example



Entity

```
entity demo is
        generic(PHYSICAL_PIN_MAP:string:="UNDEFINED");
        port(CLK:in,bit;Q:out,bit_vector(1 to 6);D:in,bit_vector(1 to 6);
                GND,VCC:linkage,bit;TDO:out,bit;TMS,TCK,TDI:in,bit);
        use STD_1149_1_1990.all;
        attribute PIN_MAP of demo:entity is PHYSICAL_PIN_MAP;
        constant DW_PACKAGE:PIN_MAP_STRING:="CLK:1," &
                "Q(6,7,8,9,10,11),D(12,13,14,15,16,17),GND:18,VCC:19," &
                "TDO:5,TMS:4,TCK:3,TDI:2";
        attribute TAP_SCAN_IN of TDI:signal is true;
        attribute TAP_SCAN_MODE of TMS:signal is true;
        attribute TAP_SCAN_OUT of TDO:signal is true;
        attribute TAP_SCAN_CLOCK of TCK:signal is (20e6,BOTH);
        attribute INSTRUCTION_LENGTH of demo:entity is 4;
        attribute INSTRUCTION_OPCODE of demo:entity is
                "BYPASS (11111),"&
                "EXTEST(0000)," &
                "SAMPLE(1100,1010)," &
                "INTEST(1010)";
```

Entity (Cont.)

```
attribute INSTRUCTION_CAPTURE of demo:entity is "0101";
attribute BOUNDARY_CELLS of demo:entity is "BC_1";
attribute BOUNDARY_LENGTH of demo:entity is 12;
attribute BOUNDARY_REGISTER of demo:entity is
    -- num cell port function safe [ccell disval rslt]
        "12 (BC_1,CLK,input,X)," &
        "11 (BC_1,D(1),input,X)," &
        "10 (BC_1,D(2),input,X)," &
        "9 (BC_1,D(3),input,X)," &
        "8 (BC_1,D(4),input,X)," &
        "7 (BC_1,D(5),input,X)," &
        "6 (BC_1,D(6),input,X)," &
         "5 (BC_1,Q(1),output3,X,000,1,Z)," &
         "4 (BC_1,Q(2),output3,X,000,1,Z)," &
         "3 (BC_1,Q(3),output3,X,000,1,Z)," &
         "2 (BC_1,Q(4),output3,X,005,1,Z)," &
         "1 (BC_1,Q(5),output3,X,005,1,Z)," &
         "0 (BC_1,Q(6),output3,X,005,1,Z)";
end demo;
```

Package

```
package STD_1149_1_1990 is
 attribute PIN_MAP:string;
 subtype PIN_MAP_STRING is string;

 type CLOCK_LEVEL is (LOW, BOTH);
 type CLOCK_INFO is record
     FREQ:real;
     LEVEL:CLOCK_LEVEL;
 end record;

 attribute TAP_SCAN_IN: boolean;
 attribute TAP_SCAN_OUT:boolean;
 attribute TAP_SCAN_CLOCK:CLOCK_INFO;
 attribute TAP_SCAN_MODE:boolean;
 attribute TAP_SCAN_RESET:boolean;

 attribute INSTRUCTION_LENGTH:integer;
 attribute INSTRUCTION_OPCODE:string;
 attribute INSTRUCTION_CAPTURE:string;
```

Package (Cont.)

```
type ID_BITS is ('0', '1', 'X');
type ID_STRING is array (31 downto 0) of ID_BIT

attribute REGISTER_ACCESS:string

type BSCAN_INST is (EXTEST, SAMPLE, INTEST,RUNBIST);
type CELL_TYPE is (INPUT, INTERNAL, CLOCK, CONTROL,
                   OUTPUT2, OUTPUT3, BIDIR_IN, BIDIR_OUT);
type CAP_DATA is (PI, PO, UPD, CAP, X, ZRRO, ONE);
type CELL_DATA is record
         CT:CELL_TYPE;
          I:BSCAN_INST;
          CD:CAP_DATA;
end record;
type CELL_INFO is array(positive range<>) of CELL_DATA;
constant BC_1:CELL_INFO;

attribute BOUNDARY_CELLS:string;
attribute BOUNDARY_LENGTH:integer;
attribute BOUNDARY_REGISTER:string;
attribute DESIGN_WARING:string;
end STD_1149_1_1990;
```

Package Body

```
constant BC_1:CELL_INFO:=(
    (INPUT,EXTEST,PI), (OUTPUT2,EXTEST,PI),
    (INPUT,SAMPLE,PI), (OUTPUT2,SAMPLE,PI),
    (INPUT,INTEST,PI). (OUTPUT2,INTEST,PI),
    (OUTPUT3,EXTEST,PI), (INTERNAL,EXTEST,PI),
    (OUTPUT3, SAMPLE,PI), (INTERNAL,SAMPLE,PI),
    (OUTPUT3, INTEST,PI), (INTERNAL,INTEST,PI),
    (CONTROL,EXTEST,PI),(CONTROL,EXTEST,PI),
    (CONTROL,SAMPLE,PI),(CONTROL,SAMPLE,PI),
    (CONTROL,INTEST,PI),(CONTROL,INTEST,PI)
);
```