TUTORIAL 1: SUNDAY AUGUST 7, 2005, 12:00-15:00

Introduction to Reconfigurable High Performance Computing

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Summary

Advances in FPGA chips and FPGA based co-processing subsystems offer the potential for substantially accelerating computationally intensive applications on current and future high performance computing (HPC) platforms through reconfigurable computing. FPGA have demonstrated substantial performance improvement in application areas such as bioinformatics, image analysis, and others. In this tutorial we will present the state of the art in reconfigurable HPC systems, design practices for such systems, and approaches to exploiting reconfigurable HPC to boost performance of your favorite application. Current challenges and common pitfalls will be discussed.

Biography

Dr. Tomko started working with custom computing systems in the mid 80s with image processing hardware accelerators at both ERIM and Synthetic Visions Systems. Since then she has gained expertise in parallel computing and FGPA based custom accelerators. Her experience with parallel scientific applications ranges from crashworthiness simulations to wireless communications simulations in collaboration with industrial and government laboratory computational groups. In addition, she has worked with industrial partners on projects in reconfigurable HPC. At the University of Cincinnati, Dr. Tomko teaches courses in high performance computing, compiling and operating systems.