VLSI Test and Validation

Midterm Test, 5/1/06

1. A *hazard-free* circuit will not produce a static hazard regardless of the signal path delays, provided only *one* input changes at a time. (a) Design a hazard-free combinational circuit for detecting prime numbers in the range of 0 to 15. The numbers are decoded as 4-bit unsigned binary numbers. Do not count 0 and 1 as primes. The output should be 1 whenever the input is a prime number. (b) Determine all undetectable single stuck-at faults in your design. (c) What is the relationship between undetectable faults and prime implicants in the K-map? (d) Is it possible to identify all/some of the undetectable faults in the design phase? (17%)

2. Given a circuit shown in Fig. 1, show the decision trees generated by D-algorithm and PODEM for g stuck-at 0, during the test generation process. (17%)

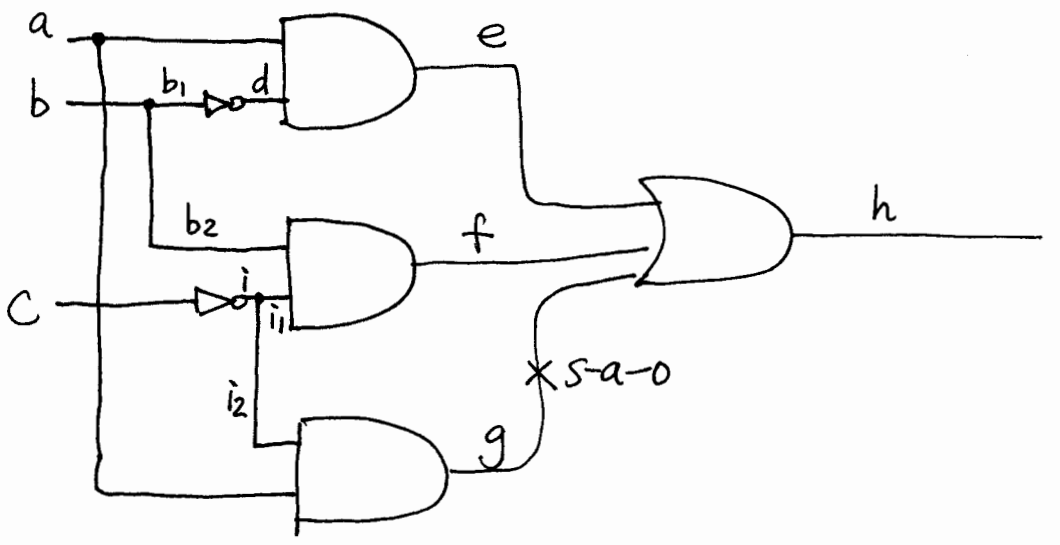

Fig. 1.

3. In Fig. 2, you have to use FAN to generate a test pattern for line 1 stuck-at 0. Your FAN cannot have any backtracking. You must use all features of FAN to show the power of this ATPG method. To help me grade your answer, you must present your solution step by step. For example:
   Step 1: To activate the fault, I assign ……
   Step 2: To propagate the fault effect through gate 100, I assign …… (17%)

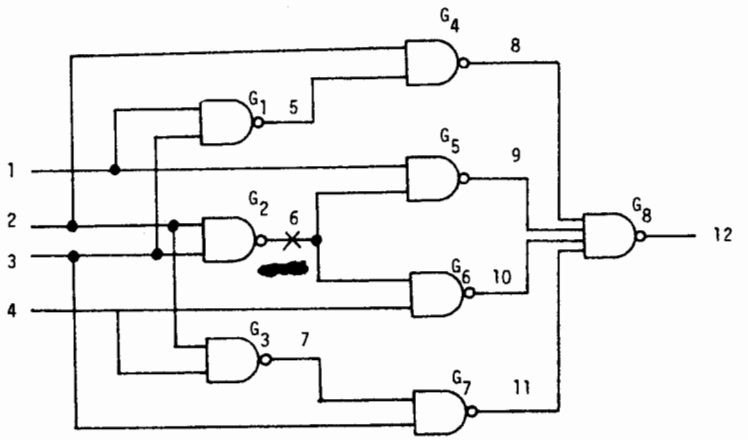

Fig. 2.

4. In Fig. 3, use concurrent fault simulation to see whether faults A/1, E/0, D/1, and J/1 will be detected when test pattern ABCD=0110 is applied. Show the process by drawing good gates and bad gates as we did in the class. Now, if the input pattern of ABCD is switched to 0101, show the change in good gates and bad gates. (17%)

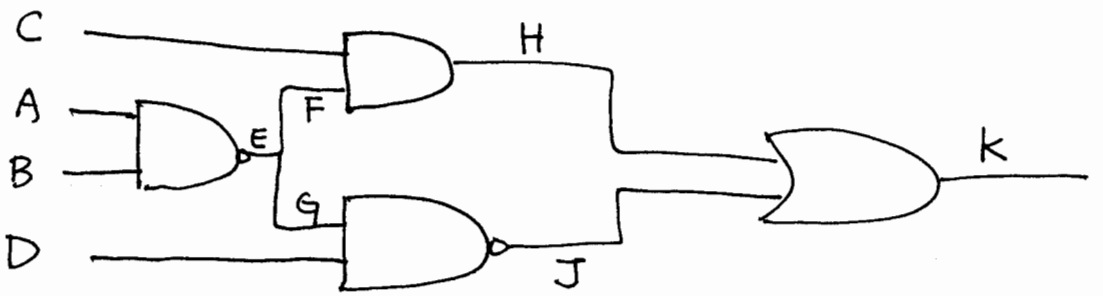

Fig. 3.

5. For the circuit shown Fig. 4, (a) use critical path tracing to determine faults detected by the test abc=111. Note that you have to first collapse faults using equivalence relation. (b) Change the logic value of input *b* from 1 to 0 and determine the remaining faults that can be detected. (16%)

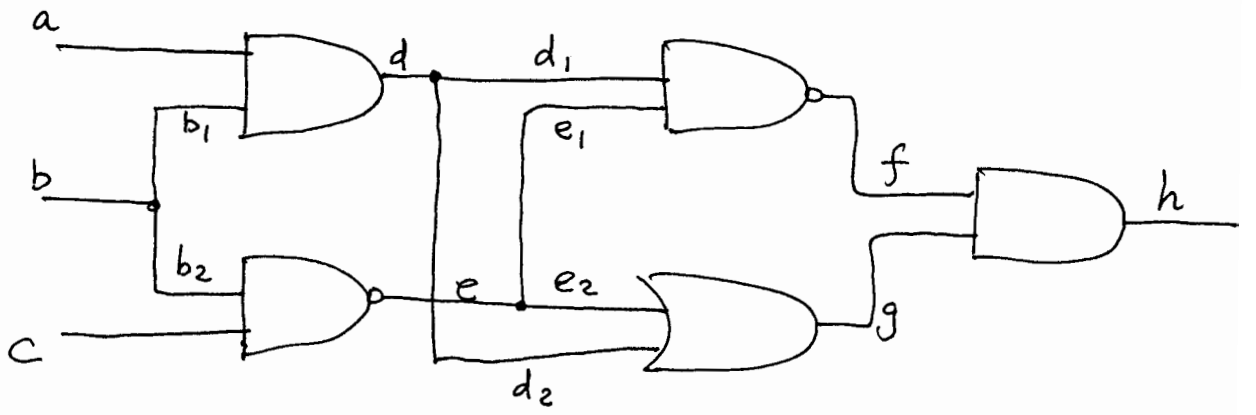

Fig. 4.

6. Given a circuit in Fig. 5, generate sequential controllability and sequential observability of each line. (16%)

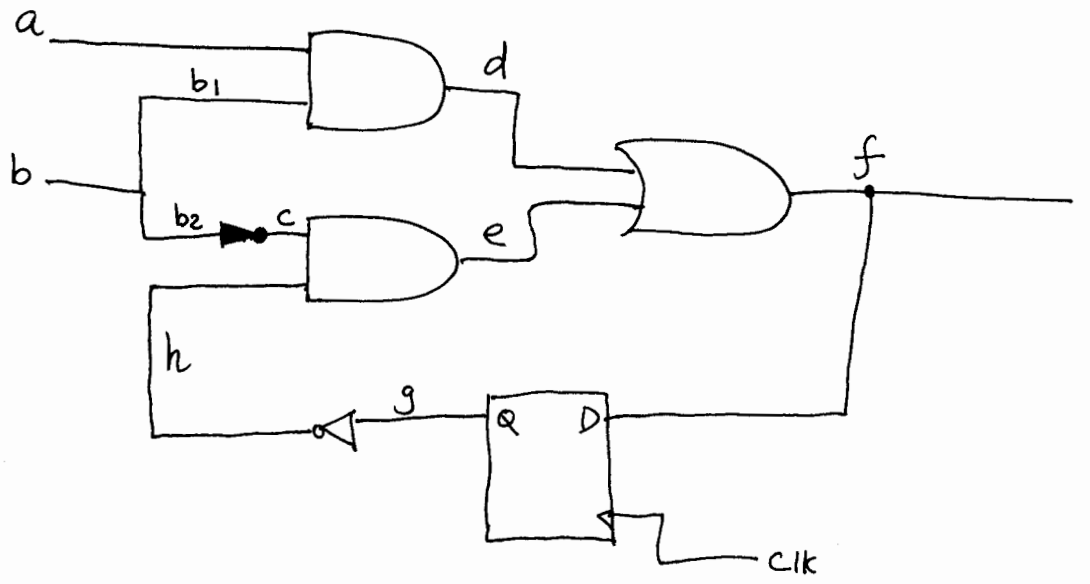

Fig. 5.