VLSI Test and Validation

Final Test, 6/6/06

1. How many test cycles are needed to shift a 4-bit test instruction into the Instruction Register of a boundary-scan architecture? Assume you start from the reset state and after the instruction is shifted in, the TAP will be in Select-DR-Scan state. Fig. 1 gives all diagrams you need for boundary scan design for Questions 1 and 2. (13%)

2. Assume the loaded instruction is an INTEST instruction. Now you are going to apply one hundred patterns to the internal logic and observe the test results. If the length of the boundary-scan register is 30, then how many test cycles will be needed to carry out the whole test procedure? Assume the internal logic is a combinational circuit, and after the test procedure, the circuit will return to the Test-Logic-Reset state. (13%)

3. There is a coupling fault called CFxyz occurring between cells in different words. Assume you have a memory array with 100 words and each word contains 1 bit only. By CFxyz, a read operation on the aggressor cell forces the content of the victim cell to a specific logic value. A CFxyz can be represented as <rx:y> where reading logic value x at the aggressor cell forces the victim cell to logic value y. There are four CFxyz faults: <r0;0>, (r0;1>, <r1;0>, <r1;1>. You are given March X as shown in Fig. 2. Which CFxyz faults can be detected by March X? Which CFxyz faults cannot be detected by March X? (13%)

Figure 2.

4. Figure 3 shows a SRAM cell which contains six transistors. Assume there is a bridge defect connecting the T terminal and the F terminal of the cell as shown, and the resistance of the bridge is R. (a) Is large R or small R easier to cause an error by this defect? Why? (b) To reduce the leakage power, we might reduce the supply voltage. Would smaller supply voltage make the cell more vulnerable to the bridge? Why? (12%) **Note: writing too much will take of risk of grading error. Just use short answers.**

Figure 3.

5. Given a circuit shown in Fig. 4, find the minimum pseudo-exhaustive test patterns. (12%)

Figure 4.

6. Answer the following sub-questions related to BIST. **(a)** Is the LFSR shown in Fig. 5(a) good for test pattern generation? Why? **(b)** In Fig. 5(b), assume the length of test sequence is m, the number of circuit outputs is n, and the length of the signature register (multiple-input signature register) is L, explain why the aliasing probability is 2^{-L}. (13%)

Figure 5(a)

Figure 5(b)

7. You are given a circuit with scan structure shown in Fig. 6(a) and 6(b), where Fig. 6(a) shows the overall scan architecture while Fig. 6(b) gives the scan cell design. Assume the circuit input is (x1, x2, x3, x4 =0010) and the scan data is 01 where 0 is the first data. Give the logic values of L1, L2, L3, L4 at time t1, t2, t3 shown in Fig. 6(c). (12%)

Fig. 6(a)

Fig. 6(b)

Fig. 6©

8. For a scan test structure shown in Fig. 7(a), assume R3 contains 6 bits and R6 contains 8 bits. How many clocks are required for each run of test application by assuming that MUX scan Flip-Flops shown in 7(b) are used for R3 and R6. Note that each test application includes: (a) scan in a test pattern, (b) apply the test pattern, and (3) scan out the response. (12%)

Figure 7(a)

Figure 7(b)