# VLSI Test and Validation
# Assignment 1

1. Consider the circuit in Fig. 1 based on the single stuck-at fault assumption.
(a) What is the number of all possible faults?
(b) Find all equivalent faults based on structural analysis. What is the collapse ratio after you perform fault collapsing (based on the equivalent faults you find)?
(c) Find all faults with dominance relationship. What is the collapse ratio after you perform fault collapsing (based on the dominance faults you find)?
(d) How many checking-point faults are in the circuit? How many of them can be collapsed by fault equivalence and fault dominance relationships?

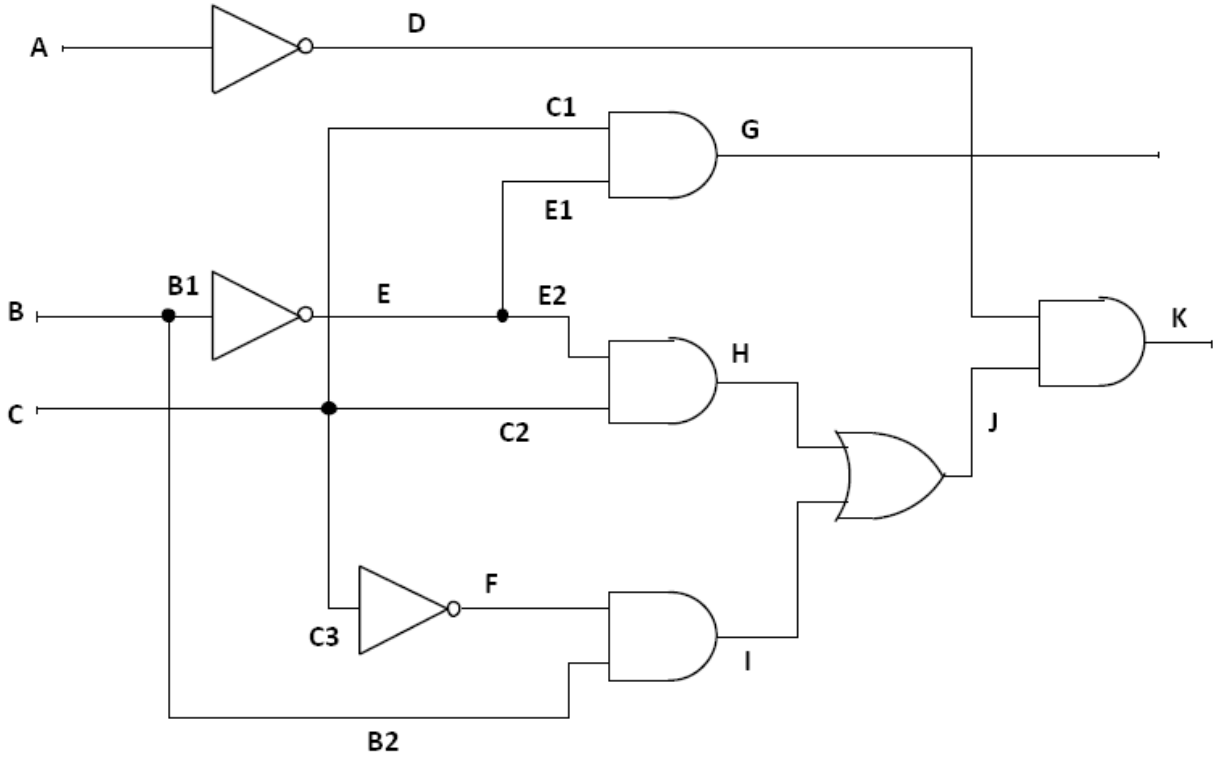


Fig. 1.

2. Fig. 2 shows the switch-level representation of a complementary CMOS gate. Assume the line marked by an X is broken.
(a) How many test patterns are required for testing this fault?
(b) Give the test pattern(s) for this fault.
(c) Is your test robust? That means, is your test safe in any condition? Give the reasons regardless of your answer yes or no.

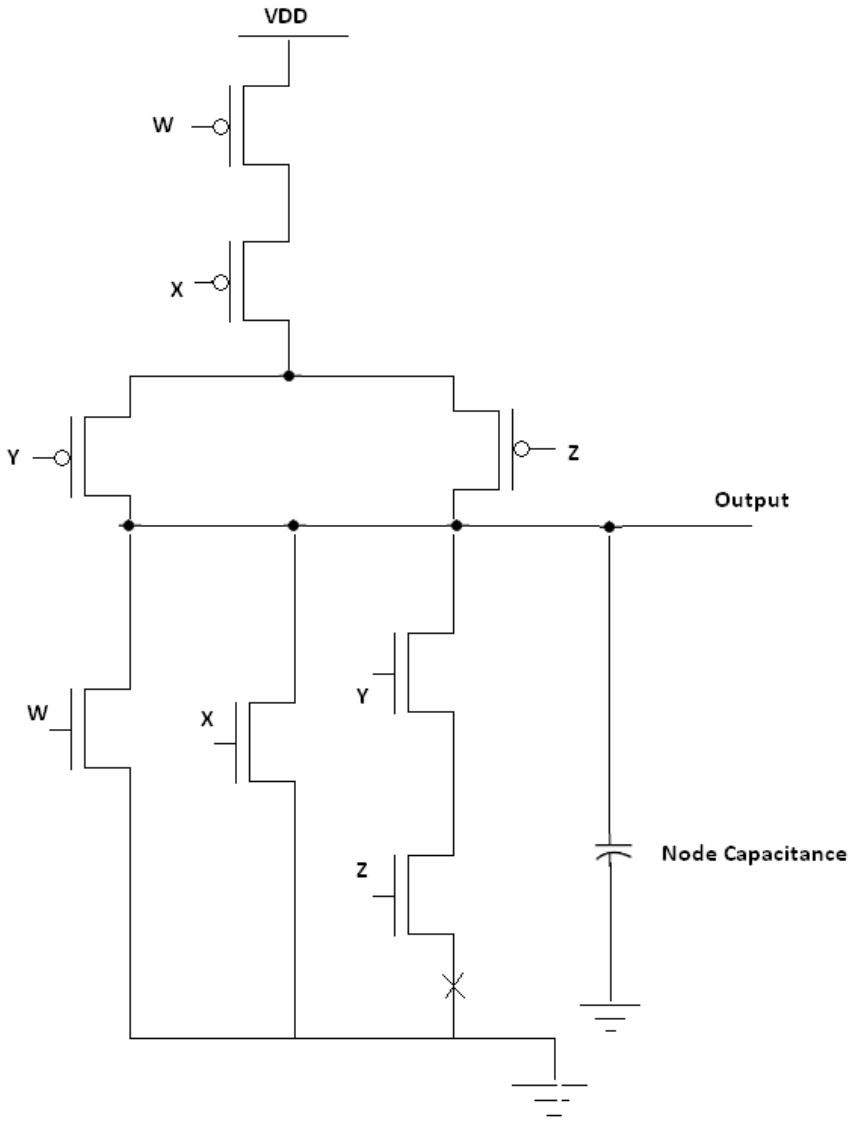


Fig. 2.