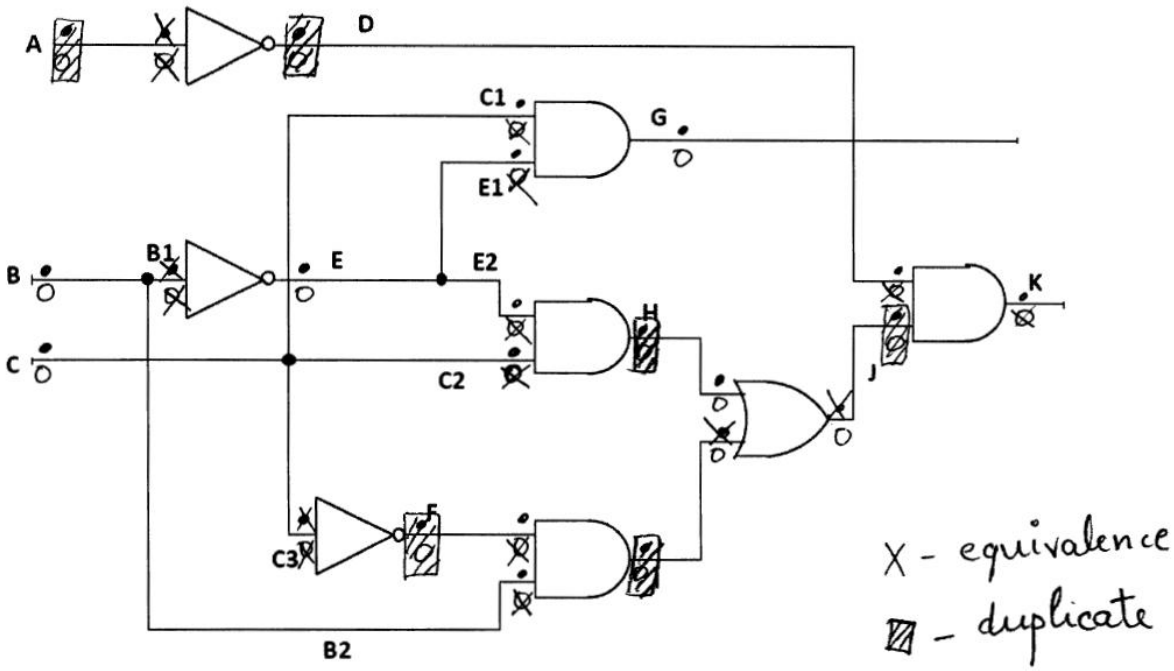
VLSI TESTING
ASSIGNMENT 1 - SOLUTION

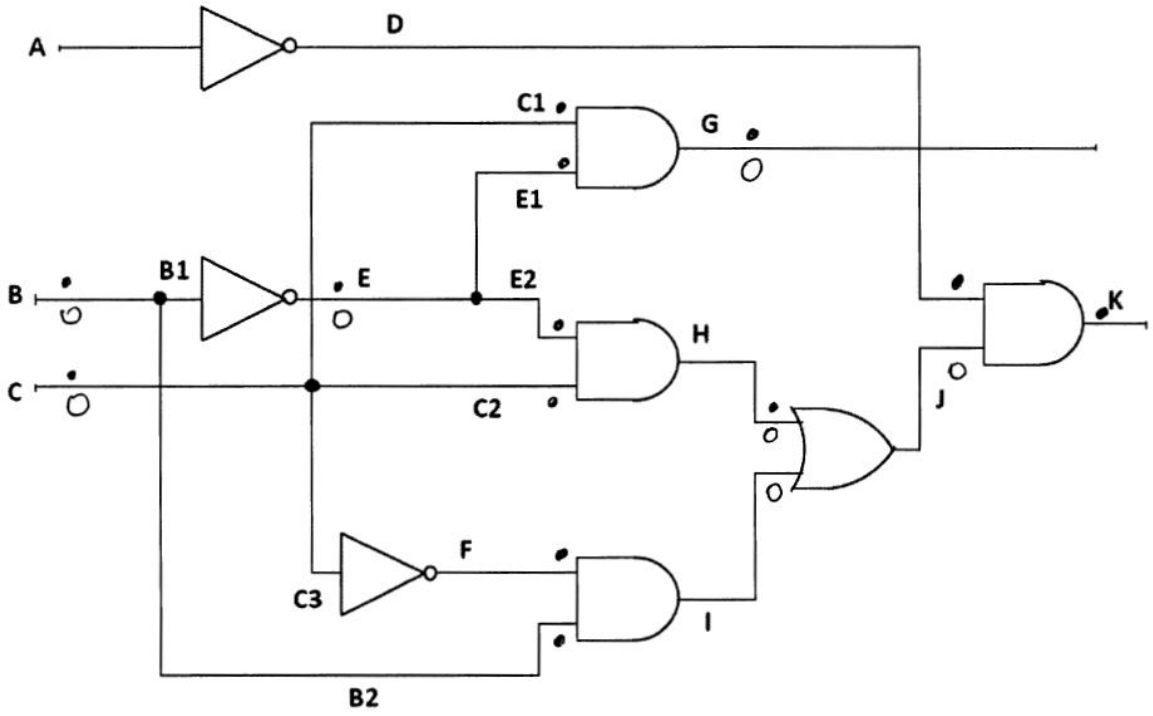
Question 1 - Solution

a) Total faults = 36

b) Fault equivalence collapsing results in 20 faults.

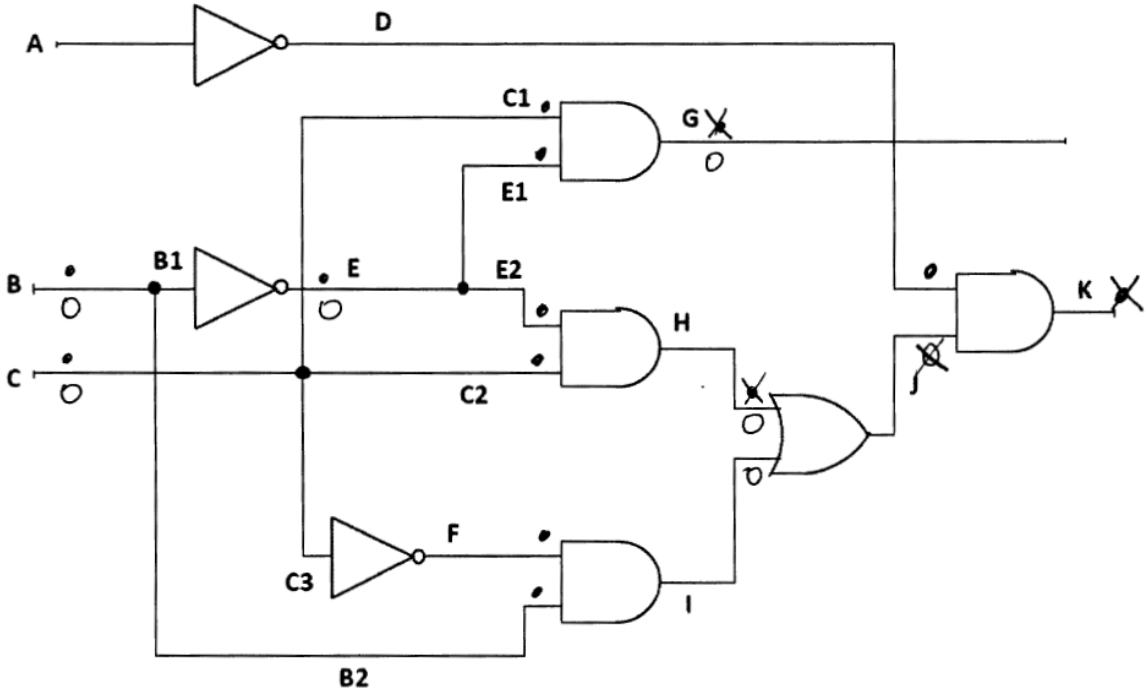
Collapse Ratio (Faults remaining after collapse) = 20/36




A
D
C1
G
E1
B
B1
E
E2
K
H
C
C2
J
F
C3
I
B2

c) Fault dominance is a superset of fault equivalence. Any two faults if equivalent, dominate each other and one of them can be removed. Hence fault dominance should be done on top of fault equivalence.

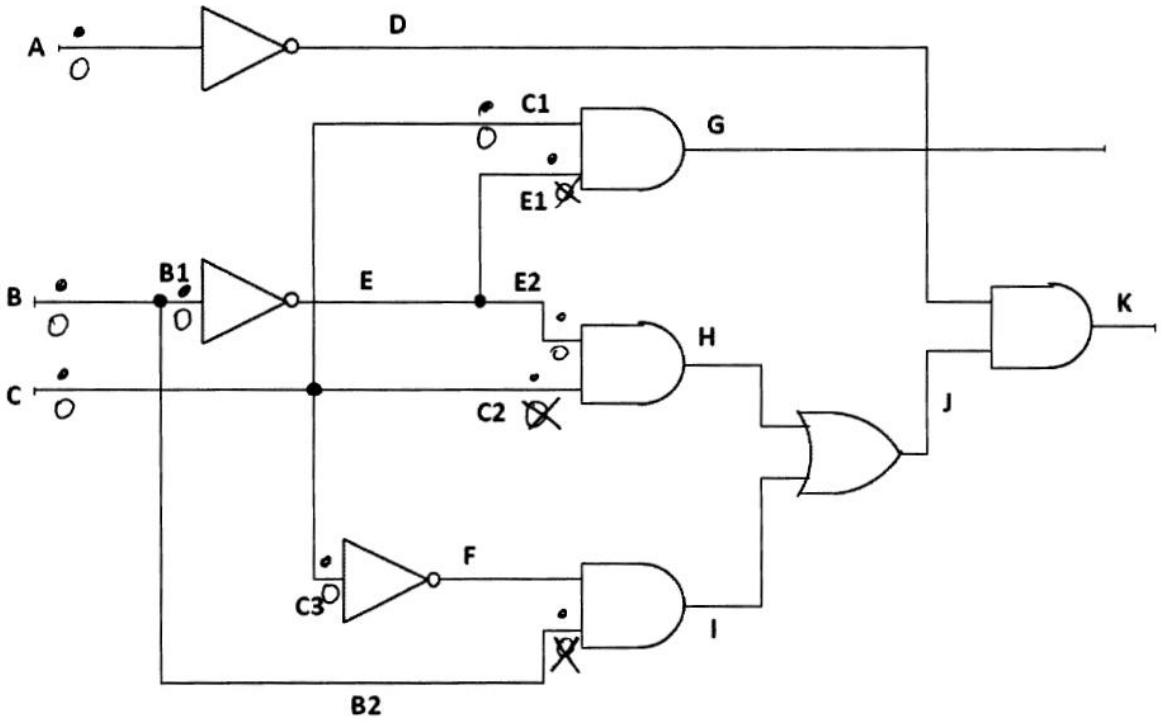
Fault dominance collapsing results in 16 faults.
Collapse Ratio (after collapse) = 16/36



d) There are 20 checkpoint faults.

Equivalence and Dominance should be checked only between these 20 faults. In equivalence and dominance collapsing at least one fault should remain.
The only faults that can be collapsed are E1 s-a-0 or C1 s-a-0 (only one of them), E2 s-a-0 or C2 s-a-0 and B2 s-a-0 or C3 s-a-1.

After collapsing 17 faults remain.



Question 2 - Solution

a) Number of test patterns -2
b) Patterns :
To charge Output = 0000, 0010, 0001
To discharge output = 0011
c) Pattern 0010 -> 0011 is robust, remaining two are not
Reason : There is a parasitic capacitance Cpar between Y and Z.
For pattern 0010, Node capacitance and Cpar are charged initially. If there is no fault, the output discharges to 0. If there is a fault, the output remains at 1 because there is no charge sharing between node capacitance and Cpar.
For patterns 0000 and 0001, Cpar is not charged initially. If there is a fault, there is a charge sharing between node capacitance and Cpar (because Cpar was initially not charged), thus the output might not be at a perfect 1. This might result in a wrong result for the test and is not robust in all cases.