# VLSI Test and Validation
# Assignment 2

1. Consider the circuit in Fig. 1. Use D -algorithm to perform ATPG for the stuck-at 1fault on line N. To simplify the ATPG process, whenever there is a choice, you first select the top input. For example, to justify M=1 in Fig. 1, you first justify I=1.

To simplify the description of the process, try to follow the steps presented in the slides as:

| Decision | Implication | Comments |
|---|---|---|

You also have to give the decision tree.

2. Repeat question 1 using PODEM.

To simplify the description of the process, try to follow the steps presented in the slides as:

| Objective | PI Assignment | Implication | D-Frontier |
|---|---|---|---|

You also have to give the decision tree.

3. Repeat question 1 using FAN.

To simplify the description of the process and to help the TA to grade your answer, you MUST list the process step by step. Here, I give an example:

Step 1: To activate the fault, we have current objective=(B1, 0).

Perform M-backtracing using (B1, 0), we assign B=0.

Perform implication: we get B2=D', B3=D', and B4=0.

D-frontier={F, G}.

You also have to give the decision tree.

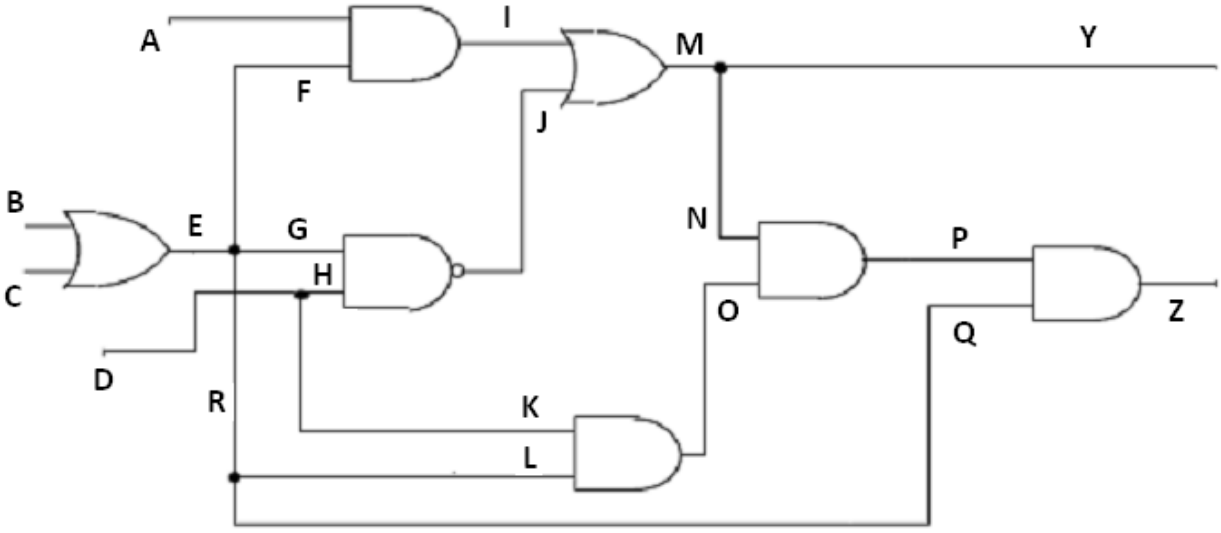


Fig. 1