VLSI Test and Validation (ECE 682)
Spring 2008
Lab - 1 to be completed by 5/24/2008

In this lab you will get familiar with the HP 16500A Logic Analysis Systems. You can find the manual in the website http://www.ece.uc.edu/~wjone/ : **Training Guide for HP Logic Analyzers.**

1. Signup for and Borrow the lab kit as mentioned in the class. Go Through the procedures described in Chapters 1-6, 9 and 11 of the "Training Guide for HP Logic Analyzers". Write a 1-page report as to whether all the exercises are done successfully. If not, note the Problems you have faced and things that didn't work etc.

2. Are these procedures extensible to test the chip you have designed during the fall quarter? **Write brief essay** on how you propose to test your chip using HP Logic Analyzer and how you might tackle the problem of testing your chip. Specifically list the potential problems you foresee with your approach and with using the testers.

3. For your mini-project from Physical VLSI Design, develop the test vectors you will be using to test the chip. Most likely, you may use scan design in which data is shifted into position through a shift register and results are shifted out. You can use strings of alternating zeros and ones to test the shift registers themselves. It remains to test the combinational logic portion of the chip ensuring a high degree of fault coverage. Use the following approach to generate test vectors for this purpose:

Define a combinational logic blob to be a collection of combinational logic gates in your chip such that the blob is fed by either primary input pins or by the outputs of registers and the blob feeds either primary outputs or registers. Your circuit can be divided into a number of combinational logic blobs which can be tested provided the test data for each blob can be loaded into its input registers and its output registers are observable at the primary outputs. Identify all the combinational logic blobs in your circuit.

- First, code each of these blobs in a form suitable to be input to Synopsys or using manual ATPG analysis. Generate test vectors for each blob ensuring maximum

fault coverage for single stuck-at faults. Make sure that your test patterns (responses) can be delivered by the scan chains you designed. Note that your circuit must be tested by test patterns derived using single stuck-at fault test patterns.

- Second, you must also identify a set of functional test patterns to make sure the correctness of functions and timing.

4. **Submit your fault model, fault list, and your test plan**. Note that you can use Synopsys (or manual ATPG analysis) to generate your test patterns if the gate-level representation of your design is available. If no gate-level representation is available, you may choose to use functional fault model which mainly checks the functions of the chip. If you will not use single stuck-at fault test patterns, you MUST give the reason in the report and also discuss with Dr. Jone. Finally, submit the test patterns and test plan you will use in testing your mini-chip, regardless of using structural test patterns or functional test patterns.