VLSI Test and Validation (ECE 682)

Spring 2008, Wen-Ben Jone

Lab - 2

Due June 8, 2008

1. Write a comprehensive test procedure for the chip using the test vectors you have generated in Lab 1, and any additional vectors that may be necessary to test the sequential logic in the chip. What is the estimated fault coverage for the entire chip using your test procedure?
2. Test the IC chip assigned to you for complete functionality using the test stations in the lab.

Your lab kit will contain a bread-board and most of the connectors and grabbers necessary. However, it is important that you take a look at the kit to make sure that you have everything you need to mount the chip on a stable fixture and connect it to the tester. Do this as soon as possible. Pay specific attention to power and clocking needs. Contact the teaching assistant if necessary.

You must test all the chips given to you. You must return at least one of them to me in good shape.

Your lab report must contain the testing methodology you have adopted, the test-vector generation strategy, number of type of faults covered, expected and actual responses from the chip, and the eventual diagnosis. Try to be as complete as possible in testing full functionality and in isolating the fault locations if any.

If you take your VLSI design report (from the physical VLSI Design Course), you must return it along with your lab report.

After you finish your chip testing, make an appointment with the TA to give her a demo. Please save your test patterns to a floppy to avoid wasting time. Note that you should give demo before you pass the test kit to the next group. Please carry your Physical VLSI report as soft or hard copy during your demo.

1. In addition to the Lab Report, you must send the TA an email message that has the subject line: TEST REPORT FOR <name of your chip> and exactly the following content:
2. REQUEST : REPORT
3. ID : <ID of your chip>
4. P-PASSWORD :
5. FAB-ID : <FAB ID of your chip>

6. P-NAME : <Name of your chip>

7. REPORT :

8.

9. <Description of the chip's function and its design.>

10.

11. <Overall testing procedure described briefly.>

12.

13. <Use of test generation system and any other software for test generation>

14.

15. <Testing of sequential logic parts>

16.

17. <Testing of combinational logic parts>

18.

19. <Any other testing done>

20.

23 <The maximum frequency that the chip can work, e.g., 50MHz>

24.

25. <Test equipment used and how it was used>

26.

27. <Result of testing, coverage achieved, whether passed/failed, and other comments>

Please do NOT include any other extraneous statements in this email report since it will forwarded verbatim to the folks sponsoring the fabrication of your chips.

You must e-mail Divya Ramakrishnan and Dr. Jone both pdf file and doc file for the test report. Also, you must pass a hard copy of the report to Dr. Jone.

Following is a sample report:

REQUEST : REPORT

ID : 38255

P-PASSWORD :

FAB-ID : N2CJCD01

P-NAME : AJHEEB

REPORT :

AJHEEB is a permutation network chip that produces a permutation of the given input based on the Control Word applied to it. It consists of mainly two logic parts; a sequential part and a combinational part....

Testing of the chip is conducted in three phases; testing the sequential part, testing the combinational part, and testing the integrated chip as a whole. Test vectors are obtained manually for the sequential part, while the Test Compiler tool by Synopsys is used to generate test vectors for the combinational part. The same test vectors are used to test the whole chip beside other test vectors generated manually.

The sequential logic part testing is performed as follows:

1. This logic part actually is a series of D-ffs connected in a shift register fashion.
2. Apply a constant input pattern to the input pins (assuming that the combinational part is fault-free).
3. Use the serial input to shift a '1-0' sequence through the shift register.
4. At each clock, observe the output if it matches the expected output.

The control word here has a "walking" '1-0' through the shift register, and if there is a flip-flop that is faulty, then the output will not change from the previous one, then we can determine the faulty flip flop. Applying the previous procedure gave no errors in the shift register.

The number of test vectors used to achieve that is 56 test vectors.

The combinational logic part testing is performed as follows:

1. Load the control word in the shift register.
2. Apply the input test vector to the input pins.
3. Observe and compare the output with the expected one.
4. Repeat the above procedure for all the test vectors.

The test vectors used in this part were generated using Test Compiler of Synopsys. The number of vectors that used is 24 vectors, and these vectors give 100 % fault coverage. Applying the previous procedure gave no faults in the circuit.

Testing the whole chip is performed as follows:

A. 1. Load a random control word in the shift register.
2. Apply input test vector that has only one bit '1' to the input pins.
3. Observe and compare the output with the expected one.

4. Repeat (1-3) for different locations of the '1'.
5. Repeat (1-4) for different control words.
6. Repeat (1-5) for input vectors that have two '1's.
7. Repeat (1-5) for input vectors that have three '1's.
8. Repeat the steps used to test the combinational logic part.

B. 1. Load specific control word that to bring the circuit in the test mode
2. Apply input vector at the input pins.
3. Observe the output if it shows the expected internal points.
4. Repeat (1-3) several times for different input vectors.

Applying the previous procedure ensured that the chip is fault-free. And the second part of the test showed that the MUX circuits, that used to multiplex some of the output pins with some internal points, function correctly. About 60 test vectors were used.
All of the chips have been tested using HP 16500A Logic Analysis Systems.....
We have tested five chips of AJHEEB and both have been shown to function correctly.