VLSI Testing and Validation (ECE 682)
Spring 2008
Lab Management Notes

1. Each lab group consists of two students. The group that designed a chip in the Fall quarter should get together again so that you can test the chip that you designed. The same grouping should continue for the entire quarter. If you were not present in Physical VLSI Design course, you need to join a group who owned a designed chip in physical VLSI course. **Please send your group names contact e-mails and Phone numbers (if available) to TA:** Divya Ramakrishnan: ramakrda@email.uc.edu **before 5/14/2008.**

2. You will need the lab kit to use a test station. There is only one kit available. There is a sign-up sheet in Rhodes 890. You have to fill in the student names of your group by 5/14/2007, so that she can finalize the slots. This lab has time slots from 5/13/2008 to 5/24/2008.

3. Typically a quota unit should be for duration of 24 hours. TA will try to allocate the quota fairly. In case of extra quota, extra quota will be allocated on a need basis or a first come and first serve basis. Extra quota will be allocated after initial allocation has been executed. Please pay attention to your email for any updates.

4. The lab kits can be checked out from Divya Ramakrishnan (805C Rhodes Hall). You can check out the lab kits at 9.00 AM, Monday – Friday, depending on your quota. When a quota expires, you must return the kits to Divya. Please do pass the kits before the stipulated time so that the next group can get it on time. The successive group should check if everything that's supposed to be in the kit is there and in good condition. Otherwise, report to TA immediately. In case of excessive damage, you are responsible for the cost of the entire kit.