Syllabus for

ECECS 682 VLSI Testing and Validation

Spring 2008

Textbooks: M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits,* Kluwer Academic Publishers, 2000, ISBN: 0-7923-7991-8.

OR

M. Abramovici, M. A. Breuer, and A. D. Friedman, Digital Systems Testing and Testable Design, Computer Science Press, 1990, ISBN: 0-7167-8179-4.

OR

L. T. Wang, C. W. Wu, and X. Wen, VLSI Test Principles and Architectures, Morgan Kaufmann, 2006, ISBN-13: 978-0-12-370597-6, ISBN-10: 0-12-370597-5.

Coordinator: Wen-Ben Jone, Associate Professor of Electrical Computer Engineering and Computer Science

Goals: Upon completion of this course, students will be able to effectively test VLSI systems using existing test methodologies, equipments, and tools.

Prerequisites: 1. 20-ECES-680, Physical VLSI Design

Topics:

1. Fault modeling
2. Automatic test pattern generation
3. Fault simulation
4. Testability measurements
5. Design for testability and scan test
6. Boundary scan testing
7. Built-in self testing
8. Memory testing
9. Case studies using CPU testing papers
10. Other most up-to-date research topics.

Computer Usage: VLSI test tools on Sun Workstations will be used for all homework and projects.

Laboratory: This course includes extensive lab experiments and hands-on usage of VLSI test equipment and tools as an integral part of the course. Lab sessions will be scheduled

each week and as necessary.

Homework assignments using test pattern generator software on the SUN workstations and testing VLSI circuits using VLSI test equipment (pattern generators, logic analyzers, etc.). These assignments cover combinational and sequential test generation, scan-paths, boundary scan, and testing an existing VLSI chip for detection and location of faults.

Grading Policy: Midterm test +Final test: 60%, Assignments + Projects: 40%.

Late Policy: 15% off for each day late.

Cheating Policy: Cheating in test - will be graded F in this course. Copying assignment – the grade will be divided by the number of people sharing the code.

Teaching Assistant: TBD

Instructor's office hours: 4:30-5:30pm, Monday, Wednesday and Friday, or anytime you can catch me. Office: Rhodes 836B, TEL:6-3319, E-mail: wjone@ececs.uc.edu

Check the website: regularly for notes, most updated announcements, assignments, or syllabus by: http://www.ececs.uc.edu/~wjone

Estimated ABET Category Content: Engineering Science: 2 credits or 50%
Engineering Design: 2 credits or 50%

Prepared by: Wen-Ben Jone, PhD **Date:** 3/31/2008